

ZEUS CALORIMETER FIRST LEVEL TRIGGER

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ABSTRACT

The design of the Zeus Detector Calorimeter First Level Trigger is presented. The calorimeter first level trigger is pipelined with a decision provided 5 μ sec after each beam crossing, occurring every 96 nsec. The trigger determines the total energy, the total transverse energy, the missing energy, and the energy and number of isolated electrons and muons. It also provides information on the number and energy of clusters. The trigger rate needs to be held to 1 kHz against a rate of proton-beam gas interactions of approximately 500 kHz. The summed trigger tower pulseheights are digitized by flash ADC's. The digital values are linearized, stored and used for sums and pattern tests. Information is sent to the Global First Level Trigger and the Level 2 Fast Calorimeter Trigger. The functionality and hardware implementation are presented in detail.

Zeus Note 89-085 (version 1.0)

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1. Introduction

The calorimeter trigger presents a challenge that is new to colliding detectors. This difficulty is not unique to the Zeus detector, but is found in other detectors planned for the SSC as well. The time between beam crossings at HERA is 96 nsec. This is too short a time for the calorimeter to read out the data and provide a trigger decision. The data are therefore kept in a pipeline and the first level trigger decision is postponed until 5 μ sec after the crossing. In order to avoid deadtime, the trigger electronics itself must be pipelined: every process in the trigger must be repeated every 96 nsec.

The Zeus calorimeter trigger must detect charged and neutral current processes. In these events the current jet(s) and lepton emerge on opposite sides of the beam axis, balancing each other in transverse momentum. The debris of the proton is emitted forward in a narrow cone (~ 10 mrad). Neutral current events are characterized by an electron and jet(s) with balanced transverse momentum (p_T). Charged current events contain jets and missing p_T . In addition, exotic processes would be distinguished by the presence of lepton(s) and jet(s) with missing p_T . The trigger rate from conventional physics is expected to be ~ 3 Hz. The most serious background is from proton beam-gas interactions in the 70 m long straight section of HERA upstream of the detector. Assuming a flux of 10^{18} protons/sec and a beampipe vacuum of 3×10^{-9} torr, this interaction rate is several hundred kHz, a significant fraction of which eventually cause signals in the detector. The first level trigger rate needs to be held to 1 kHz.

The calorimeter trigger is based on several quantities. These are the total energy deposited in the calorimeter, the sum of transverse energy, missing p_T , and the number and energies of jets, isolated electrons, and isolated muons. The Zeus calorimeter consists of depleted uranium plates interleaved with plastic scintillator. The scintillator plates form towers which are read out on two sides with wavelength shifter bars, light guides and photomultipliers. The calculations required for the calorimeter trigger include summing all of the pulseheights recorded in the photomultipliers every 96 ns. In addition, calculation of the transverse energy and missing p_T requires algebraically summing pulseheights multiplied by geometric factors. The detection of jets requires preservation of individual tower information that would be lost in a global sum. The detection of an electron requires evidence of electromagnetic energy. This is done by comparing energy deposited in the first interaction length of the calorimeter with that deposited later on a tower by tower basis.

2. Calorimeter First Level Trigger Overview

The photomultiplier signals are combined into analog supertower sums. Due to the geometry of the detector, these supertowers vary considerably in dimensions. For the sake of conceptual explanation, the ideal supertower described has the most common geometry. This ideal supertower has a cross sectional area of 20 cm square longitudinally divided into EMC and HAC sections. The EMC section is divided transversely into four 5 cm x 20 cm sections, while the HAC section is divided into two 20 cm square longitudinal sections. Each section is read out through a wavelength shifter on both the right and left sides. Therefore, two phototubes read out each section. The most common variation on this geometry is a supertower with an undivided front HAC section read by 2 phototubes in place of the 4-part EMC section read by 8 tubes. A side view of an ideal supertower is shown in Figure 1.

Generally, there will be 4 EMC sections, 5 cm x 20 cm apiece, read out by 2 PMT's each, for a total of 8 PMT's, which are summed for the supertower EMC output. These are followed by 2 HAC sections, each 20 cm square, read out by 2 PMT's each, for a total of 4 PMT's, which are summed for the supertower HAC output. There are 460 supertowers in the Forward Calorimeter (FCAL), of which 264 have EMC sections. The remaining 196 FCAL supertowers have a HAC

section in place of the EMC section and its pulseheight is included in the HAC sum. There are 448 supertowers in the Barrel Calorimeter (BCAL), all of which have EMC sections. There are 452 supertowers in the Rear Calorimeter (RCAL), of which 262 have EMC sections, which have 2 sections, 20 cm x 20 cm apiece, read out by 2 PMT's each, for a total of 4 PMT's.

The 1360 total calorimeter supertowers each provide a HAC sum and 974 of the supertowers also provide an EMC sum. The tower geometry is set by the positions of the EMC supertower sections. These are projected back to HAC sections which are then summed to match the EMC projection. In regions of overlapping coverage from the FCAL to BCAL or BCAL to RCAL, there is further summing of EMC supertower sections. The result is that the FCAL and RCAL are each divided into 4 7x8 supertower regions, and the BCAL is divided into 8 7x8 supertower regions. The geometry of these regions is described in the section on Assignment of Trigger Crates and Supertowers. Each supertower has a HAC sum and an EMC sum, yielding 1792 analog sums. These are then digitized by two 8-bit flash, ADC's (FADC) with a two different gains, to cover the dynamic range properly, and multiplexed to registers. Each FADC is matched to a memory lookup table that stores the linearized, pedestal-subtracted pulseheight for each FADC response placed in the registers.

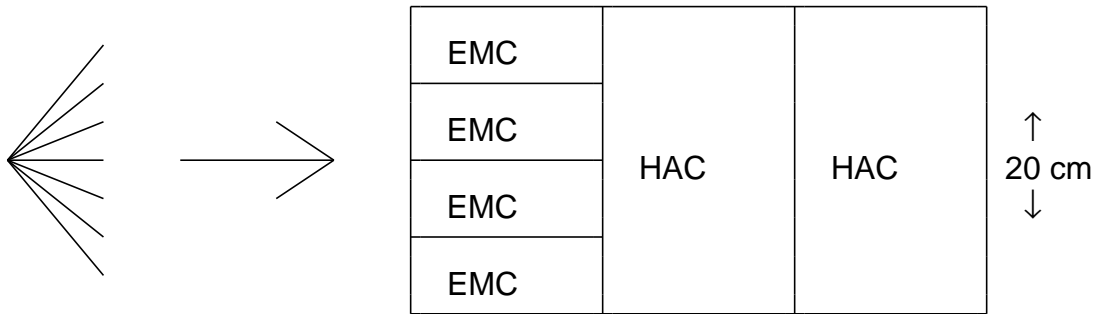


Figure 1. A particle from an interaction entering an ideal supertower.

The structure of the calorimeter trigger is severely constrained by the necessity to repeat each step and to pass processed information to the next step every 96 nsec. The trigger must first form the total energy, transverse energy and missing p_T sums. Given an EMC or HAC supertower sum of energy E_i located at polar angle θ_i and azimuthal angle ϕ_i , the sums may be formed from the quantities E_i (total energy), $E_i \sin \theta_i$ (transverse energy) and the components $E_i \sin \theta_i \cos \phi_i$ (missing E_x) and $E_i \sin \theta_i \sin \phi_i$ (missing E_y). The digitized HAC and EMC pulseheight from each of the 896 supertowers is stored in a register, multiplied by a lookup table containing these four geometric factors and injected into an adder tree summing network with the different geometric factors. The network sequences through the 4 EMC and then the 4 HAC sums of all supertowers for each crossing every 96 nsec. A sequence of 8 energies, summed through the adder tree emerges for each crossing at the end of the tree. Since the same summing network is used to compute all 8 of the sums, only one is needed. The summing network keeps 8 bits of data with a 9th overflow bit.

The formation of jet and isolated electron triggers in a pipelined fashion is considerably more complicated than making sums. The trigger system uses tables to make local tests on the amount of energy in an individual supertower against six jet energy thresholds. In addition, supertowers are tested for minimum ionizing pulseheight and "quiet" pulseheight (less than one-fifth minimum ionizing), and overflows. The ratio of HAC to EMC energy is also tested. The results of these tests are encoded in a series of bits and are passed forward with the energy sums to a search table that looks for matches with desired patterns. Regional energy sums and tests are

also made at this stage. The final information from the tests and sums is forwarded to the Global First Level Trigger (GFLT), which compares the calorimeter information with that of the other detector elements in making the final trigger decision.

In summary, the overall organization of the Calorimeter First Level Trigger begins with the left and right supertower sums from the front end Analog Cards. Each set of left and right sums is combined into a single sum on the Trigger Sum Card. These analog sums are then sent to the Trigger Encoder Cards in the Rucksack. The Trigger Encoder Cards digitize, linearize, sum and test these signals and send them to Adder Cards in the same crate. The Adder Cards continue the summation process and search for patterns among the test results. The Adder Cards forward their results to the Trigger Processor Crate, which makes the final decisions on this information to forward to the Global First Level Trigger Box (GFLT). Upon receipt of a GFLT, the stored EMC and HAC energy values for each supertower from the triggering crossing are shipped from each TEC card to the Fast Clear, which decides whether to request an abort of the GFLT based on calorimeter information. The logical organization of the Calorimeter First Level Trigger is illustrated in Figure 2.

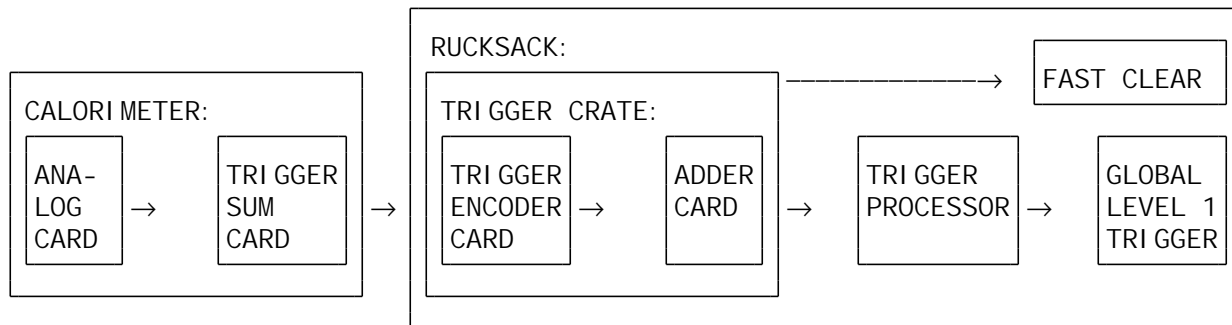


Figure 2. Logical flow and location of Calorimeter First Level Trigger.

3. Trigger Sum Card

The front end electronics is composed of Analog Cards servicing 12 photomultipliers connected to either the right or left sides of 2 supertowers. The Analog Card services 4 supertowers in the case where the supertowers have front HAC sections (HAC0) with only 2 tubes in place of EMC sections that have 8 tubes. There are four left or four right outputs for each front end Analog Card. For the majority of supertowers, these would be set through jumpers to give two sets of EMC (4 tubes) and HAC (2 tubes) sums for the two supertowers. In locations where a HAC0 section exists in place of an EMC section, the card outputs 4 sets of HAC sums (3 tubes each) for 4 supertowers. In the RCAL, the Analog Cards have 8 outputs apiece, to produce a HAC and EMC sum for every (approximately 20 cm x 20 cm) supertower.

The Trigger Sum Card (TSC) sits in the calorimeter backbeam area adjacent to the front end Analog Cards. It has 8 current inputs (4 left and 4 right) and generates 4 outputs. The cables from the Analog Card to the TSC are the same length throughout the FCAL, BCAL and RCAL. The only exception is where additional cable length is added to compensate for the faster tubes used in the FCAL EMC towers. The result is that all FCAL, BCAL and RCAL TSC's receive their signals simultaneously. Each TSC output consists of two amplifiers capable of driving a shielded twisted pair cable in differential mode. A single TSC services the left and right sums for two supertowers. The TSC sums each of the left and right sums for each supertower to produce two sums each for two supertowers with both EMC and HAC sections, and four HAC sums for four supertowers without EMC sections. In order to facilitate combinations of HAC cells in the FCAL and RCAL regions close to the BCAL, the TSC has internal jumpers that allow up to four of its

eight total inputs to generate a single output. In these cases, one or more of the four output channels are unused. In most locations, two input channels are summed in one output channel. However, in regions of complex geometry, the TSC is used to directly combine the left and right sides of two HAC (four inputs) sections in a single output sum.

The phototube gains are set so that 1 GeV of energy in a single FCAL section produces a charge of 3.65 pC on each of the two phototubes attached to it, and 1 GeV of energy in a single BCAL section produces a charge of 5.30 pC on each of the two phototubes attached to it. This means that when the left and right phototubes attached to a section are summed, the total charge produced per GeV of deposited energy is 7.3 pC in the FCAL and 10.6 pC in the BCAL.

Each front end Analog Card sums all of the hadronic and electromagnetic phototube signals in each supertower and outputs 1/20 of the total hadronic and electromagnetic phototube current for either the left or right side of the supertower. The charge delivered to the TSC for a minimum ionizing particle (Q_{mip}) is 1/20 of the total section (sum of left and right PMT's) pC/GeV given above times the energy deposited by a minimum ionizing particle (E_{mip}), where E_{mip} is given in Table 1. The energy deposited in the HAC is the sum of both HAC sections. The maximum charge delivered to the TSC (Q_{max}) is 1/20 of the total section pC/GeV given above times the maximum energy that can be deposited in a section (E_{max}), where E_{max} is 400 GeV for the FCAL and 100 GeV for the BCAL. In addition, there are a few BCAL supertowers which have FCAL sections summed with BCAL sections. For the BCAL sections in these supertowers, the gain is set so that E_{max} is 400 GeV. The TSC can drive at most a signal of 2 V on its output cable to the Trigger Encoder Card (TEC). This sets the gain of the TSC at $2000 \text{ mV}/Q_{\text{max}}$. The currents and charges for minimum ionizing and maximum energy, along with the gains of the TSC for the various sections of the calorimeter are listed in Table 1. The minimum ionizing particle currents (I_{mip}) and maximum currents (I_{max}) in Table 1 are computed from their corresponding charge assuming a 20 nsec rectangular pulse. The digitization scales of the low gain and high gain channel FADC's in the TEC are computed using the information that the high gain scale for all calorimeter sections is 0 to 12.5 GeV. This gives a high-to-low gain ratio of 32 in the FCAL and 8 in the BCAL.

Table 1. Total HAC and EMC energy deposited in supertowers for various regions of the calorimeter, along with total (left + right) input charges and currents (5% of total after PMT gain listed) to the Trigger Sum Cards (TSC) for these regions. The gain and output of the TSC are listed along with the scale and digitization resolution in GeV per Least Significant Bit (LSB) at the Trigger Encoder Cards (TEC).

Value of Quantity for:	BEMC	BHAC	FEMC	FHAC
E_{mip} (Supertower Total in MeV)	321	1360	363	2268
PMT Gain (S'tower Total pC/GeV)	10.6	10.6	7.3	7.3
Q_{mip} (TSC input, pC)	0.17	0.72	0.13	0.82
Q_{max} (TSC input, pC)	53	53	146	146
I_{mip} (TSC input, μA)	8.5	36	6.6	42
I_{max} (TSC input, μA)	2650	2650	7300	7300
TS Gain (mV/pC)	37.7	37.7	13.7	13.7
TS Output for Q_{max} Input (Volts)	2.0	2.0	2.0	2.0
mV/GeV at TEC input	20.0	20.0	5.0	5.0
GeV/LSB in TEC Low Gain Channel	0.391	0.391	1.56	1.56
MeV/LSB in TEC High Gain Channel	48.8	48.8	48.8	48.8

Each TSC channel has two current inputs (left and right halves) which are summed, and drives one twisted pair cable at its output. The Trigger Sum Card integrates the sum of the two

input currents. These currents are transmitted from the front end Analog Cards to the Trigger Sum Card on 50 Ω coaxial cable. Each input line is connected to an emitter, which is biased with a 1mA dc current drawn by the front end Analog Card. The low impedance of the emitter provides a suitable termination point for the series 50 Ω resistor. The left and right currents may then be summed by connecting the collectors. 80% of the input current flows through a 100 Ω resistor into the summing node of a Comlinear CLC400 operational amplifier.

The total charge associated with the current is converted to an output voltage by feedback capacitance. The capacitance used will differ for the BCAL and FCAL due to their different gains. The other 20% of the input current flows into a 100 nsec lumped constant delay line. It constitutes a voltage signal that mimics the shape of the current signal delivered initially to the CLC400. 100 nsec later, this voltage signal drives a current source comprised of a transistor and associated resistors. The ac component of this current source is then fed through a coupling capacitor into the CLC400 summing junction. The charge that was initially stored on the feedback capacitor is swept out, restoring the baseline at the amplifier output. A schematic of a prototype TSC circuit is shown in Figure 3.

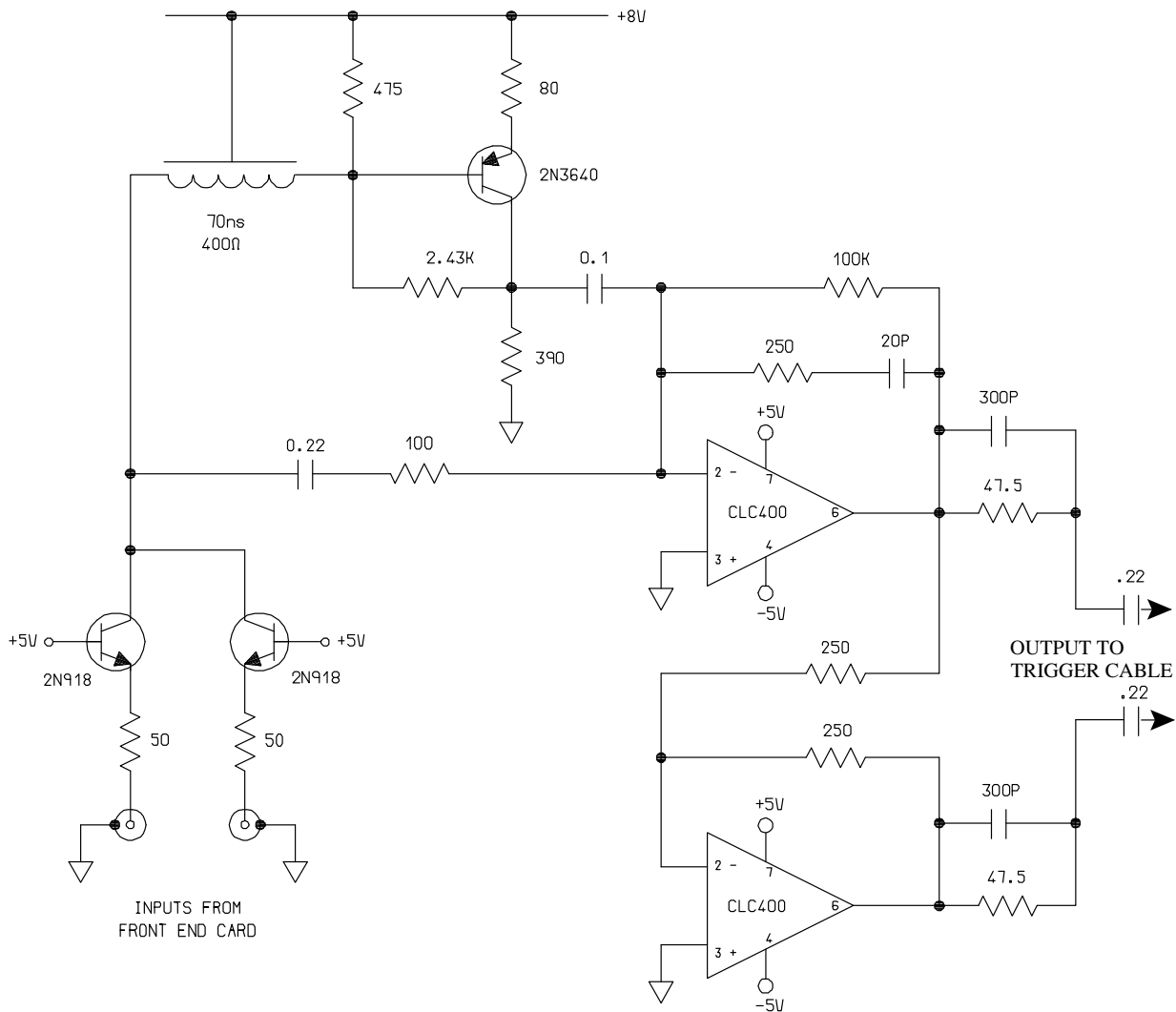


Figure 3. Circuit Diagram of One Channel of the Trigger Sum Card.

The sums are then sent out through approximately 60 m of cable with this differential driver circuit to the TEC's in the rucksack. The driver can generate a maximum differential voltage of 4V (2V per amplifier). This voltage is immediately divided in half by two 47.5 Ω resistors in series with the 94 Ω resistance of the cable, generating a differential voltage of 2 V at the cable input. The cable chosen is individually screened twisted pair flat cable. This cable is used by the OPAL collaboration at CERN and passes CERN safety tests. Two twisted pairs are needed for each supertower. Each pair occupies an area of 6 x 3 mm². The cable has a measured line-to-line characteristic impedance of 94 ohms with a variation of $\pm 1 \Omega$ from pair to pair and a line-to-shield Z of half that. The propagation and dispersion delay variation from pair to pair has been measured to be 1% and 2%, respectively. The 47.5 ohm resistors on the TSC dampen the back-reflections and the receiving side of the cable at the TEC is also properly terminated. The percentage of a signal remaining at subsequent crossings at the TEC front end after 60 m of cable is shown in Figure 4.

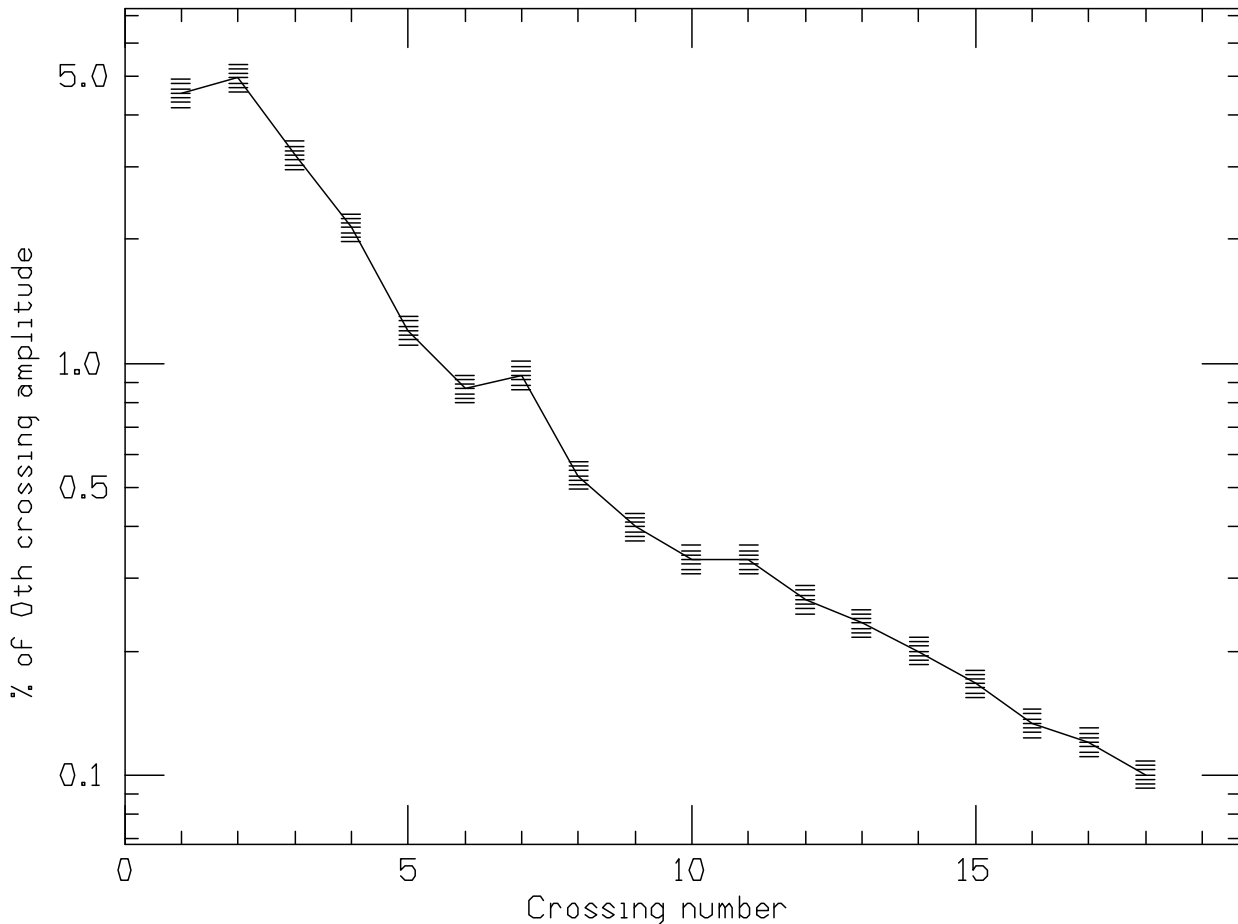


Figure 4. Percentage of original signal from the TSC remaining for subsequent crossings at the TEC front end after 60 m of Trigger Cable.

The TSC contains a serial interface which connects to a command cable. This cable carries commands that cause the TSC to turn off either the left or right input sum. The purpose of this is to compensate for the failure of a left or right signal. If, for example, the right sum of a particular supertower section were very noisy, it would be shut off, while the TEC would multiply the gain of the supertower section by 2, to compensate for the loss of pulseheight from the right sum.

Under normal conditions, all sums are turned on. Turning power off and on causes all channels to turn on. The interface and command structure that drives this operation will be done in the same manner as the rest of the slow control for the Zeus experiment. The serial control signals will be generated in a VME crate in the Rucksack, which is connected via Ethernet to the equipment computer.

The TSC also applies a threshold to each pair of left and right inputs. This threshold is set at 45% of the electron threshold applied at the TEC. The threshold voltage is provided on a cable input to each TSC. The threshold voltage is set by a DAC at the module cable bulkhead. This DAC is controlled by the same command cable as the TSC input on/off circuitry. If either the left or right signal exceeds the threshold, while the other does not, a logic signal is generated for the time that the disagreement is present. The signals on an individual TSC card are ORed together. These signals are called the TSC Veto because they are designed to veto electron signals resulting from noise on an individual EMC PMT. If this noise is the correct amount, it will pass the electron threshold on the TEC and since the tower HAC section and the surrounding tower HAC and EM sections will be quiet, this will pass as an isolated electron. We have provided for bringing out the TSC veto signals individually. They will also be combined for each half module into a single half-module veto signal, which is sent directly to the calorimeter trigger processor in the Rucksack. There the signal is deglitched and latched with the appropriate crossing and used to veto the isolated electron signal in one of the 16 CAL regions. The information is also passed to the Fast Clear, where it also vetos isolated electron signals.

The TSC veto signals are produced by every pair of summed inputs. Since the veto signals are issued for both HAC and EMC sections, they can be used to prevent other triggers caused by signals from noise sources. The source of veto signal, whether an EMC or HAC channel, is not distinguished on an individual card. It is assumed that the noise rates are sufficiently low so that accidental vetos of real triggers are not a problem. A channel that is this noisy will have its input to the TSC shut off. The vetos that result from a HAC channel may be useful in preventing a large HAC discharge from being identified as a seed tower for a jet.

The cables for the TSC include: 1 8-pair TSC Cable for every 2 Trigger Sum Cards or fraction thereof, 1 8-pair Veto Cable for every 8 Trigger Sum Cards or fraction thereof, and 1 8-pair Control Cable for each Calorimeter Module. The Control Cable consists of a Clock line (input), 2 Data Lines (1 input, 1 readback), 2 Veto Sum Lines (One per half module), one Data Latch, and 2 Control Lines reserved for Future Use. The Veto Cable carries back individual veto signals from each TSC card. The TSC Cables carry the analog signals from the sum of left and right PMT's to the TEC's. Since the signals entering the TSC arrive at the same time throughout the FCAL, BCAL and RCAL, the only length difference required between the FCAL, BCAL and RCAL cables is that needed to remove global differences between the FCAL, BCAL and RCAL. Therefore, all FCAL cables are of the same length, as is the case for the BCAL and RCAL. The numbers of cables required are described in Table 2.

Table 2. *Total cables and cables by module type between the Calorimeter Trigger Electronics in the Rucksack and the TSC cards on the Calorimeter Modules. Listed are the calorimeter type, module designation, number of Analog Cards, number of TSC's, number of TSC, veto, and control cables, total cables per module, number of this type of module, and total cables per module type.*

Cal.	Module	# FEC	# TSC	TSC Cbl	Vet Cbl	Ctr Cbl	Total/M	# Mod	Total
BCAL	All	14	7	4	1	1	6	32	192
FCAL	1B,1T	10	5	3	1	1	5	2	10
FCAL	1,2	22	11	6	2	1	9	10	90
FCAL	3,4	18	9	5	2	1	8	4	32
FCAL	5	16	8	4	1	1	6	2	12
FCAL	6	12	6	3	1	1	5	2	10
FCAL	7	8	4	2	1	1	4	2	8
FCAL	8	6	3	2	1	1	4	2	8
RCAL	1T	4	4	2	1	1	4	1	4
RCAL	1B	6	6	3	1	1	5	1	5
RCAL	1,2	12	12	6	2	1	9	8	72
RCAL	3,4,5,6	10	10	5	2	1	8	8	64
RCAL	7	8	8	4	1	1	7	2	14
RCAL	8	6	6	3	1	1	5	2	10
RCAL	9	4	4	2	1	1	4	2	8
Total									539

4. Trigger Encoder Card: Front End

The function of the Trigger Encoder card is to receive and digitize the analog trigger sum signals. The card produces a linearized energy value for each of these signals. It stores these energy values in a 64-element FIFO so that they can be sent to the Fast Clear upon receipt of a Global First Level Trigger (GFLT). It tests the energy values against six different thresholds. It tests for a "quiet tower", i.e. a value of energy consistent with noise, for a "minimum ionizing" energy level, and for overflows (energy beyond the input dynamic range). It also tests the ratio of EMC to HAC energy to see if the energy deposition is consistent with an electromagnetic shower. It forwards the results of these tests to the Adder Card that resides in the same crate. Finally, it multiplies the energy values by geometric factors to compute total Energy, E_T , E_X , and E_Y for each supertower EMC AND HAC, and sums up these EMC and HAC energies separately for transmission to the Adder Card.

The organization of the front end of the Trigger Encoder Card is shown in Figure 5. The signal is received by 2 amplifiers with high and low gain. These two amplifiers each drive a FADC which digitizes the signal. These digital results are then used as input to two memory lookup tables that produce linearized energies in the various ranges described below. A schematic picture of one quarter of a Trigger Encoder Card is shown in Figure 6.

Up to 16 signals from Trigger Sum Cards may be received by a single Trigger Encoder Card (TEC) that resides in the Rucksack. However, only 8 of these may be independently digitized. The basic organization is that the EMC and HAC sums from 4 supertowers are digitized by each TEC. In those cases where two HAC sums were grouped with an EMC sum, the card digitizes the HAC sums in pairs from up to 8 supertowers. Each of the channels on the TEC has 2 input connectors. These are received separately and combined at the input to a single amplifier. This allows the combination of 2 separate HAC supertower sums before amplification. In addition,

this provides the option of having a single TEC service both the EMC AND HAC sums for 8 supertowers instead of 4.

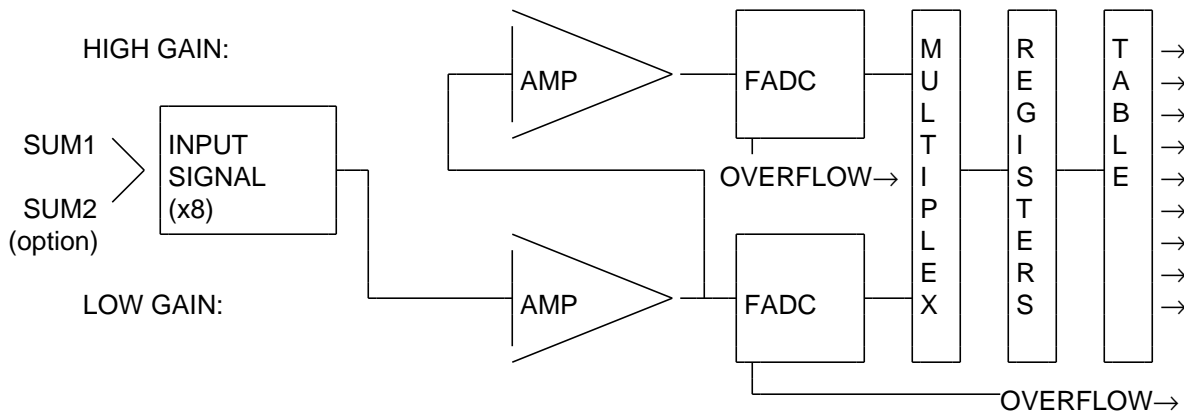


Figure 5. Organization of the Trigger Encoder Card front end.

Each input signal (single or combined) is brought through one amplifier for the low gain, and through a second for the high gain. The amplifiers employed are video amplifiers with 2 nsec propagation delays: the Comlinear CLC500 with gains between 1 and 8 is used for the low gain channels, and the Comlinear CLC501 with gains between 7 and 50 is used for the high gain channels. The gains of these amplifiers are set so that full scale corresponds to a 2V output into 50 Ω . The input scales of the TEC are described in Table 1.

Table 3. Full scale value in GeV of high and low gain channels required for different calorimeter supertowers. EMC AND HAC sections are listed separately. The maximum range (in GeV) needed for the sum of EMC and HAC sections is also listed. The value in channel number for on a 12-bit linear scale corresponding to this range is given for the "quiet" and "minimum ionizing" supertower tests. (Based on a Monte Carlo study by Allen Caldwell, Columbia University).

Full Scale (GeV):			High Gain		Low Gain		Total	Channel Number	
Detector	Tower	θ°	EMC	HAC	EMC	HAC	SUM	QUIET	MIN.
FCAL	1	5	12	12	400	400	400	2	12
	3	15	12	12	300	300	400	2	15
	5	24	12	12	200	200	250	3	24
	11	24	12	12	100	100	150	5	40
BCAL	3	40	12	12	100	100	100	8	48
	33	90	12	12	75	75	75	11	64
	53	129	12	12	50	50	50	16	96
RCAL	8	132	12	12	40	40	45	18	80
	5	145	12	12	40	40	40	20	90
	1	172	12	12	40	40	40	23	100

The energy ranges found in various sections of the calorimeter are described in Table 3. The trigger system covers these ranges by setting full scale for all high gain EMC and HAC channels to $E_{MAX}=12.5$ GeV, and setting up two low gain scales, one for FCAL and the other for BCAL and RCAL. The FCAL TECs have a low gain channel with full scale at $E_{MAX}=400$ GeV, and the BCAL and RCAL TECs have a low gain channel with full scale at $E_{MAX}=100$ GeV. Since the least significant bit for each of these scales is $E_{MAX}/256$, the high gain scales are .05 GeV/bit, and

the low gain scale is 1.6 GeV/bit for the FCAL and 0.4 GeV/bit for the BCAL and RCAL. The offsets for all the high gain channel Comlinear amplifiers are set together by a single DAC, as those of the low gain channels are set by a second DAC. This allows independent adjustment of the FADC pedestals for the high and low gain channels.

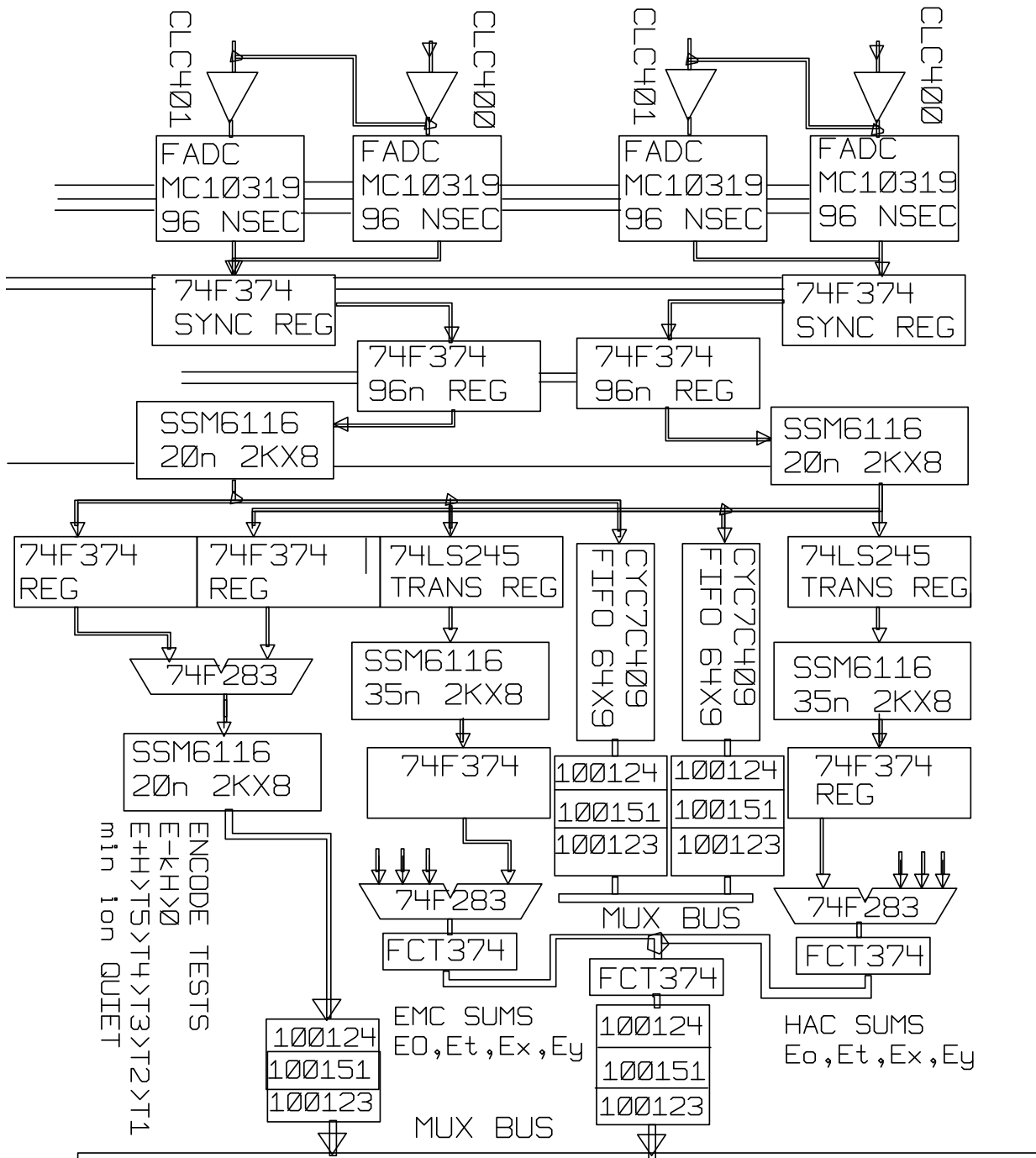


Figure 6. Schematic layout of one quarter of a TEC.

After amplification, each signal is digitized by an 8-bit FADC, Motorola 10319. The FADC's are clocked by a specific 96 nsec period clock (FADCLK) whose phase is set to sample the incoming signal correctly. The overflow bit of the high gain channel FADC drives the select

on a multiplexer. If the overflow bit is low, the value of the high FADC is written into the register. If the overflow bit is high, the value of the low FADC is written into the register. In either case, the value of both the high gain and low gain FADC overflow bits are also written into the register. This register is clocked with a 96 nsec clock (SYNCLK), whose phase is set to synchronize the FADCLK clock with the 96-nsec clock (96CLK) driving the entire trigger system in synchronous lockstep. There are 10 bits of data, the 8 bits of FADC data (either high or low) and the high and low channel overflow bits, which are written into the register. The contents of this register are sent to a second register that is clocked by the 96CLK clock. The TEC contains a programmable DAC which can place voltages on the FADC inputs. This is used to test linearity and pedestals. For diagnostic purposes, the high gain channel FADC can be disabled with the DAC offset, so that the low gain channel value will be always multiplexed out. This enables determination of the ratio of gains of the high to low channels.

The contents of the 10-bit synchronized register (8 bits of either high or low gain FADC data plus two bits of high and low gain FADC overflow) form the address presented to a TTL memory (Linearization Memory) organized into two pages. An 11th bit of address, changing state every 48 nsec, switches the memory between the two pages.

The first page of the Linearization Memory converts the raw FADC pulseheight and range information into a calibrated energy on two different 8-bit scales depending on whether the high or low gain FADC data was used. This is determined by the high gain FADC overflow bit (0 if high gain was used, 1 if low gain was used). When the high gain FADC data is converted, it is placed on a scale of $12.5 \text{ GeV}/256 = 49 \text{ MeV/bit}$, and when the low gain is converted, it is placed on a scale of $400 \text{ GeV}/256 = 1.6 \text{ GeV/bit}$ for the FCAL and $100 \text{ GeV}/256 = 0.39 \text{ GeV/bit}$ for the BCAL and RCAL. The value of true energy corresponding to each FADC value is recorded as an 8-bit word at the address of the FADC value. This energy is fully corrected for gain, pedestal and nonlinearities. It is determined by comparison with the calibrated calorimeter analog data as processed through the data acquisition system. The 8 bits of energy, along with the high gain FADC overflow bit are placed in a 9-bit register for the geometric factor memories that feed the E , E_T , E_x , and E_y values to the adder trees. The contents of this 9-bit register are also placed in a 64x9 FIFO (CYC7C409), which is clocked forward by 96CLK, and stored for use by the Fast Clear.

The second page of the Linearization Memory contains 8-bit words that include one bit ("MI") indicating the section (either HAC or EMC) has an energy that is consistent with that deposited by a minimum ionizing particle. The second bit indicates that the section has an energy less than that which is consistent with a minimum ionizing particle, and therefore is tagged as quiet ("QU"). One scheme for setting the QU and MI bits is shown in Table 4. The remaining six bits place the energy on a compressed (nonlinear) scale between minimum ionizing and the maximum possible energy that could be deposited. The value of the six bits ranges between 0 and 62. The value of 63 is reserved for when the low gain FADC overflow is set, where the 6 compressed energy scale bits are set to 1. One compressed energy scale that satisfies these requirements is $\{\ln(\text{Energy in GeV})\} * \text{CESF}$, where CESF (Compressed Energy Scale Factor) is given in Table 4. The values chosen to set the QU and MI test bits are allowed to be different for the EMC AND HAC sections of a single supertower. The values chosen to set the compressed energy scale bits are allowed to be different between supertowers based on the dynamic range of energy depositions. The layout of the TEC front end linearization and tests for one supertower (1/4 of a TEC) is shown in Figure 7.

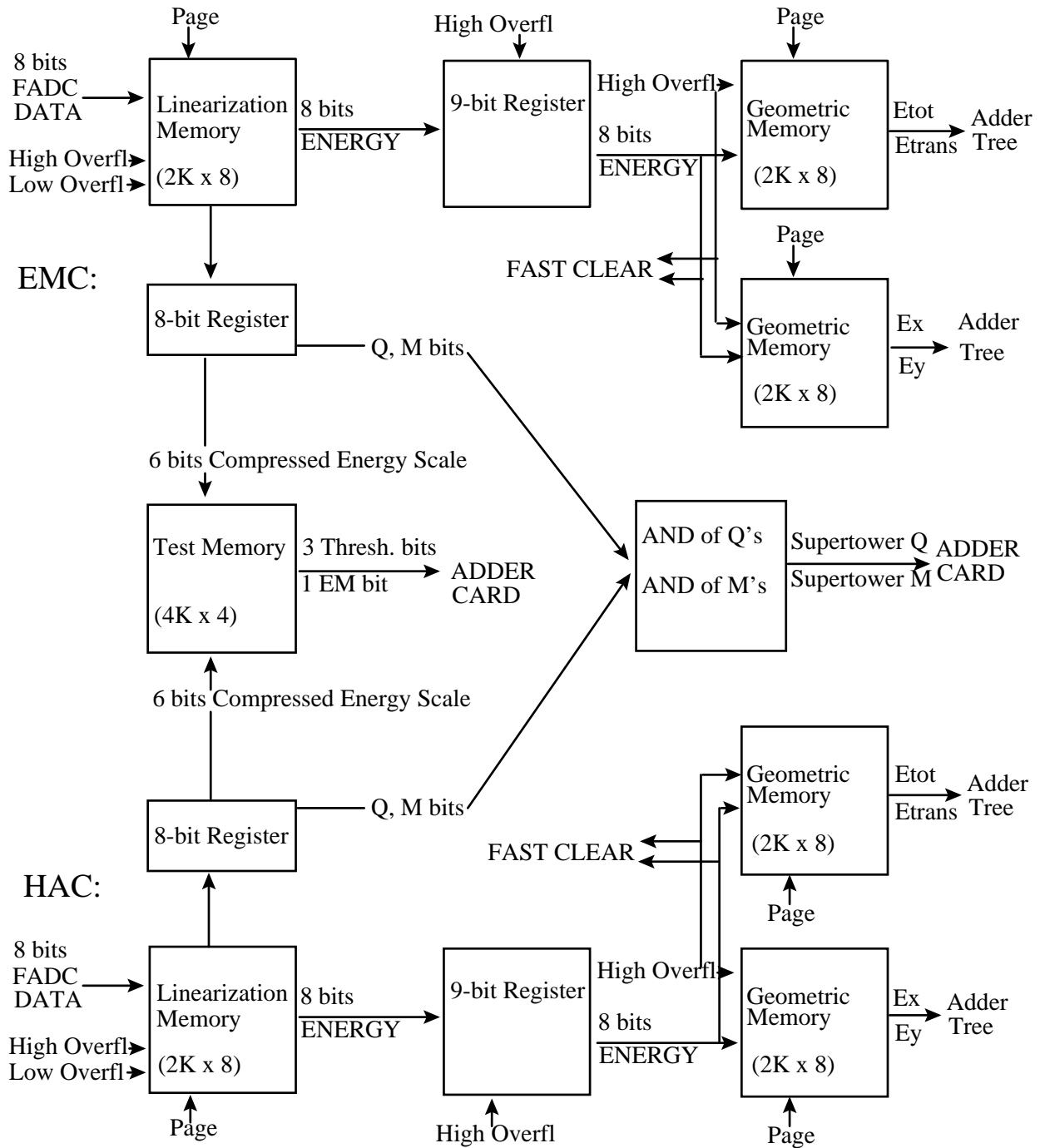


Figure 7. Layout of TEC front end linearization and tests.

Table 4. Values used to set the QU and MI test bits. The energy in high gain channel number of a minimum ionizing particle on a scale of 48.8 MeV/LSB is listed first, followed by the maximum channel number for which the QU test is passed, the minimum channel for which the MI test is passed, and the maximum channel for which the MI test is passed. These cuts implement for each calorimeter region the requirement: $E(QU) < 0.2 * E_{mip} < E(MI) < 2.0 * E_{mip}$. Finally, the Compressed Energy Scale Factor (CESF) used for the largest dynamic range towers in the FCAL (400 GeV full scale) and BCAL (100 GeV full scale) is listed.

Value of:	BEMC	BHAC	FEMC	FHAC
E_{mip} (channel number)	7	28	7	46
Quiet (maximum channel)	1	5	1	9
Minion (minimum channel)	2	6	2	10
Minion (maximum channel)	13	56	15	93
CESF (for maximum energy scale)	13.5	13.5	10.3	10.3

The contents of the 9-bit register (8 bits of energy and 1 bit of high gain FADC overflow) form an address that is presented to two TTL memories (Geometric Factor) organized into two pages apiece. The high gain FADC overflow is used as the ninth bit of address. A 10th bit of address, clocked at 48 nsec, switches between the two pages. The first and second pages of the first memory contain E and E_T values, respectively, while the first and second pages of the second memory contain E_X and E_Y values, respectively. The values in these memories are stored in 8 bits. For the total energy sum, the scale is set for all channels at 400 GeV/256 = 1.6 GeV/bit. Since the maximum value of E_T is 75 GeV, the E_T (Esinθ) values for all channels are placed on a scale of 75 GeV/256 = 0.29 GeV/bit. Since the E_X (Esinθcosφ) and E_Y (Esinθsinφ) values are signed numbers ranging between -75 GeV and +75 GeV, they are expressed in 2's-complement notation on a scale of 150 GeV/256 = 0.58 GeV/bit. The output pages of these memories are used as inputs to two parallel adder trees, clocked at 48 ns. The first page of the first memory provides the E for the first adder tree, and 48 nsec later, the second page provides the Esinθ. The first page of the second memory provides the Esinθcosφ to the second adder tree, and 48 nsec later, the second page provides the Esinθsinφ.

All of the above memories may be downloaded with the the value of the address for each address everywhere. This has the effect of passing through the input value multiplied by 1. This procedure is only used for diagnostic and calibration purposes and is designed to output the raw FADC values. The memory has additional input registers attached which are used to download the values above, as well as to inject test data at this point into the TEC. This allows the raw data from the FADC's to be propagated through the board without alteration by the linearization, geometric and test factors contained in these memories. The choice of normal operation, downloading constants, or testing is set by flags provided by the control logic described below.

5. Trigger Encoder Card: Sums

There are four parallel TTL adder trees employed on the TEC. One pair of parallel adder trees sums up E, E_T, E_X, and E_Y from the 4 HAC sections serviced by one TEC card, and another pair sums up the 4 EMC sections. In either pair (HAC or EMC) the first adder tree uses the two pages of the four TTL memories that contain the E and E_T values for either the HAC or EMC section. At the beginning of the 96 nsec cycle, the four E values are read in, and after 48 nsec, the four E_T values are read in. The second adder tree of the pair uses the two pages of the four TTL memories that contain the E_X and E_Y values for either the HAC or EMC section. At the beginning of the 96 nsec cycle, the four E_X values are read in, and after 48 nsec, the four E_Y

values are read in. The energy scale for the total energy sum is 1.6 GeV/bit (400 GeV full scale) and the energy scale for the other sums is 0.3 GeV/bit (75 GeV full scale). These values are combined separately for EMC and HAC sections to make the total energy, E_T , E_X , and E_Y sums. The TTL memories that send their output to the adder trees are shown in Figure 7. A diagram of one of the two pairs of adder trees on a TEC is shown in Figure 8.

Each of the input memories to the adder trees has its 2 pages clocked out to a TTL register (74FCT374) following it with a 48 nsec clock (TTL48CLK) generated from the 12 nsec clock. Each of two the registers transfers its values, clocked by TTL48CLK into a parallel TTL adder (74F283) where they are summed with the values from the adjacent supertower section of the same type (HAC or EMC). The 8-bit results are clocked by TTL48CLK into a second register (74FCT374). The contents of this register are transferred to another TTL parallel adder by TTL48CLK and are summed with the contents of the sum of the other 2 supertowers. The 8-bit results are transferred into a fast TTL register (74FCT374A) under 48CLK. At each stage of addition, the carry is kept as a 9th bit that is ORed with the carry from subsequent additions. This constitutes the overflow bit. At the first stage of addition, the low gain FADC overflow bits of the input channels are also ORed with the carry bits. There is one overflow bit kept for the E and E_T sums. The overflow for the E_X and E_Y sums is ignored. The E_T sum overflow is used to indicate an overflow condition for the E_X and E_Y sums. The final results of the sums are 9 bits total: 8 bits of data and an overflow bit. Since the E_X and E_Y are signed numbers, they are kept in 8 bits of 2's complement format, with the overflow bit ignored.

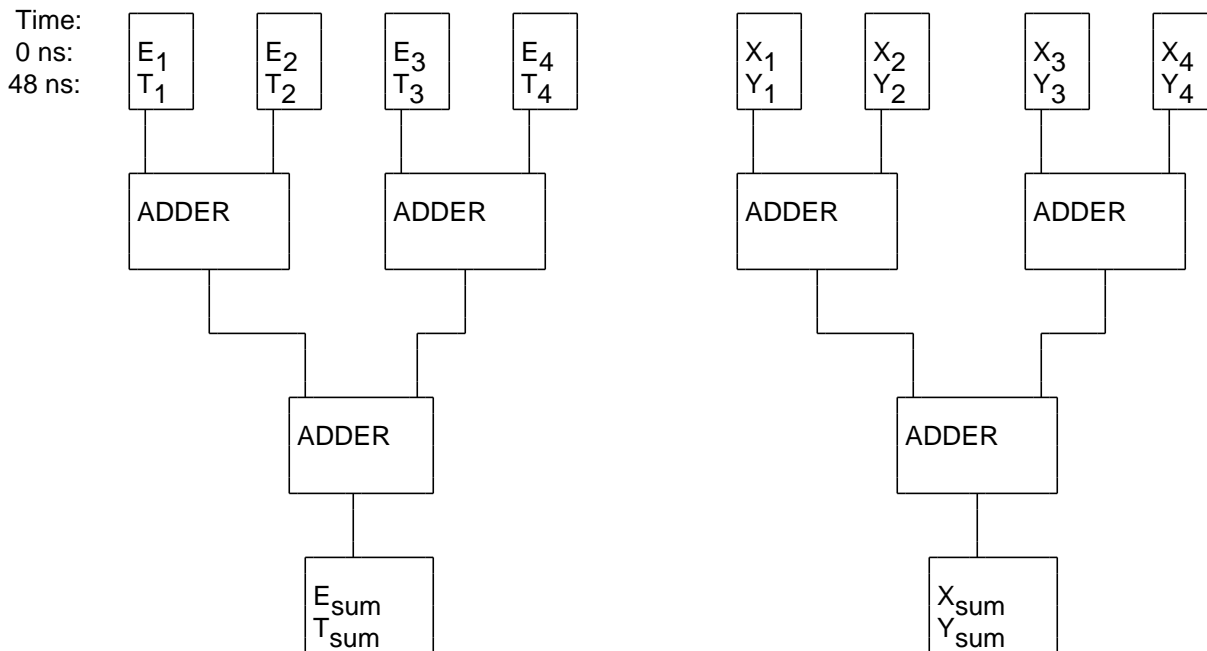


Figure 8. Half (either HAC or EMC part) of the adder tree network on each TEC. E_i represents the total energy in the supertower section, T_i is $E_i \sin \theta_i$ (transverse energy), X_i is $E_i \sin \theta_i \cos \phi_i$ (E_X) and Y_i is $E_i \sin \theta_i \sin \phi_i$ (E_Y).

New results from the 2 HAC sum networks and the 2 EMC sum networks are placed in 4 fast TTL registers every 48 nsec. A set of 4 12-nsec long enable pulses (EMCSUM1, HACSUM1, EMCSUM2, HACSUM2) causes each of the TTL registers to send forward its data in sequence (twice per register per 96 nsec beam crossing) to a single fast TTL register. The

register contents are clocked forward with a 12 nsec TTL clock (TTL12CLK) through a TTL-to-ECL translator (100124) to an ECL 6-bit shift register (100151), which clocks its results out under a 12 nsec ECL clock (ECL12CLK) to 7 sets of ECL drivers (100123) of 9 lines apiece. One of these sets of drivers is enabled and sends the data out over 9 bus lines on the backplane at a 12 nsec rate. The format and bus structure are described below. Each of the 7 TEC's in a half of a Trigger Crate broadcasts data on one of the 7 sets of lines. The set is selected under software control.

6. Trigger Encoder Card: Tests

The test encoding circuitry uses the QU, MI and compressed energy scale bits from the EMC and HAC sections of a single supertower. These are produced by the second page of the linearization memory as detailed above, and shown in Figure 7. These 8 bits are placed in one register for each section. The tests made on a specific supertower are "quiet", minimum ionizing, electromagnetic energy, overflow of the low gain channel, and six different energy thresholds. There are 4 test circuits on each TEC. Each circuit makes all of the tests on one supertower. The bits for the 4 supertower EMC and HAC sections are brought together simultaneously to each of the 4 test circuits. The energy threshold and electromagnetic tests are made by a memory with 12 bits of address composed of the 6 compressed energy scale bits from the EMC section register and the 6 compressed energy scale bits from the HAC section register.

Each test memory address location has a four bit word consisting of three bits of energy threshold test (T1, T2, T3) and one bit of electromagnetic test (EM). The three bits of energy threshold test contain the result of testing the sum of the EMC and HAC energies against six energy thresholds, ranging from 000 (exceeding no threshold) to 110 (exceeding the sixth threshold). One set of thresholds is 6.3, 12.5, 25, 50, 100, and 200 GeV for supertowers with FCAL EMC's, and 1.6, 3.1, 6.3, 12.5, 25, and 50 GeV for supertowers with BCAL or RCAL EMC's. If either of the low gain overflow bits has been set, the 6 bits of compressed energy scale will be all 1's. This address will cause all three output threshold bits to be set to one. This data indicates a low gain channel overflow.

The EM bit is set by a comparison of the EMC and HAC section energy. For example, the table can require that the EMC energy be five times greater than the HAC energy and that the EMC energy be at least 5 GeV. If either set of compressed energy scale bits indicates a low gain FADC overflow, the EM bit is set false, regardless of whether it would have passed the EM test otherwise. As in the case of the energy threshold test bits, the EM bit can be set by any arbitrary function of the 6 EMC and 6 HAC compressed energy scale bits that form the table address. The function can be changed by downloading different values into the table. The test memory has additional input registers attached which are used to download its values as well as to inject test data at this point into the TEC. The choice of normal operation, downloading constants, or testing is set by flags provided by the control logic described below. The QU and MI bits from the EMC and HAC section registers are combined in separate QU and MI AND's, resulting in supertower QU and MI bits.

The results of the tests are contained in 6 bits accumulated in a TTL register (74FCT374) after 96 nsec. The bits are the "quiet" test bit (QU), the minimum ionizing test bit (MI), the electromagnetic test bit (EM), and the three energy threshold test bits (T1, T2, T3). There are 4 of these TTL registers, one for each supertower. A set of 4 24-nsec long enable pulses causes each of the TTL registers to send forward 6 total bits in sequence to a single TTL register. The register's contents are clocked forward by TTL24CLK through two TTL-to-ECL translators (100124), wired in parallel, to an ECL register (100151), which toggles between the 100124's and clocks its results out under ECL12CLK to 8 sets of ECL drivers (100123) of 3 lines apiece.

One of these sets of drivers is enabled and sends the data out over 3 bus lines on the VME backplane at a 12 nsec rate. The format and bus structure are described below.

7. Trigger Encoder Card: Data and Control Structure

Each Trigger Encoder card is assigned one of 7 sets of 13 lines on the J3 bus or the J2 bus. The choice of set is made by setting the enable on ECL drivers (100123). There are 7 enable lines taken from a 3 to 8 bit decoder (100170) which is driven by three lines (SELPOR) set by external control. Each of these 7 lines controls one of the seven sets of drivers. The ECL drivers send 13 bits of data every 12 nsec on the backplane busses with 50 Ω lines terminated at each end. Each 13 bit word includes one of the 7 4-supertower sums (total Energy, E_T , E_X , and E_Y for each supertower EMC AND HAC) in 9 bits and 3 out of the 6 total test bits for each supertower. The TEC puts a bit on a 13th line that toggles from high to low with each word that is placed every 12 nsec on the bus. This toggling is used by the Adder Card to verify that the TECs are sending data. The TEC data format is illustrated in Table 5.

Each TEC recognizes commands that carry the address of the card. The card address is contained in 5 bits on VME lines A19-23. The VME address and data lines are buffered through registers (74ALS241). The A19-A23 bits are checked against values set on a dip switch in a comparator (74ALS520). A match sets the SLVN line high on the VME interface (SC868172), which sets the SLVSELN so that the command is enabled. A command is written into the command register (74FCT374), which is an 8-bit data register with a specific address, with a VME write command. When the address of the command register is set on the address lines (A1-3 set to 0 and A14, A17, A18 set to 1) and lines A19-23 contain the address of the card, the VME write line enables the data on data lines D0-7 to be written into the command register. The 6 commands correspond to values 1 through 6 set in the lowest 3 bits of the command register. This is done to avoid values of all 0's or 1's (0 or 7), which are the most likely to be set by a malfunction, from being recognized as valid commands. The commands are decoded into 5 separate output lines. One line for each command is set on, while the others remain at zero. The upper 3 bits of the command register contain the number selecting which of the 8 sets of 13 output lines is used for the output data from the TEC (SELPOR). These bits are decoded into 8 separate lines that are the enables on the drivers connected to the data lines used on the J2 and J3 busses.

Table 5. *Output bit structure on a 13-bit wide bus, clocked at 12 nsec so that the data is contained in 8 words sent out in 96 nsec. The energy sums of total energy for EMC AND HAC, transverse energy for EMC AND HAC, and the x and y components of energy for EMC AND HAC are summed over 4 supertowers and contained in 10 bits of each of the eight words as shown. XXI stands for the XX test bit from supertower I, where XX = QI, MI, EM, E1, E2, E3 as described in the text. The elapsed time is in nsec.*

Word	Time	Bt1	Bt2	Bt3	Bt4	Bt5	Bt6	Bt7	Bt8	Bt9	Bt10	Bt11	Bt12
1	0	←	-	-	EMC TOTAL SUM	-	-	-	-	→	QU1	MI1	EM1
2	12	←	-	-	HAC TOTAL SUM	-	-	-	-	→	T11	T21	T31
3	24	←	-	-	EMC TRANS SUM	-	-	-	-	→	QU2	MI2	EM2
4	36	←	-	-	HAC TRANS SUM	-	-	-	-	→	T12	T22	T32
5	48	←	-	-	EMC X SUM	-	-	-	-	→	QU3	MI3	EM3
6	60	←	-	-	HAC X SUM	-	-	-	-	→	T13	T23	T33
7	72	←	-	-	EMC Y SUM	-	-	-	-	→	QU4	MI4	EM4
8	84	←	-	-	HAC Y SUM	-	-	-	-	→	T14	T24	T34

The commands are INIT, SETW, SETR, TEST, and RUN. The INIT command sets zero into the front end memory address lines, zeroes the FIFO, and sets the input and output of the tests and sums to zero. The SETW command enables the writing of the memories that are used to linearize the FADC value, set the geometric factors for the adder tree and perform the tests. The SETR command enables the reading of these memories. The TEST command enables the writing of test data directly into the registers in front of each of the memories that linearize the FADC data, set the geometric factor for the adder tree and perform the tests. The purpose is to set in patterns of test data, to check the circuit functions and particularly to check the memories for defective bits. The RUN command is set on for normal operation.

The memory lookup tables are written when the command register contains the SETW command. This enables access to the 4 memory select lines (TYPE): LINM selects the linearization memory, GMA and GMB select each of the 2 geometric factor memories that feed the adder tree, and TSTM selects the memory used by the tests. The selection of memory type is placed on lines A17-18 (LINM=00, GM1=01, GM2=10, TSTM=11). The SETW command also allows the VME write line to set the write enable (WENAB) to all the memories by setting their output enables high. The memories in a particular EMC or HAC supertower of the 8 on the card are selected by the tower select line (TOWER), which is decoded from VME address lines A14-16. These address lines contain the numbers 0-7 for Tower 1 HAC (0), Tower 1 EMC (1), through Tower 4 EMC (7), respectively. The memories are written by the write strobe (WSTROB) which is generated by the VME interface IC (SC868172). The WSTROB is derived from an AND of 96CLK, SLVSELN, VME write, TYPE, and TOWER. The address of the memory that is to be written into is taken from the VME address bits A1-13 (the LSB is stripped off). These lower 7 bits are written into a counter, while the upper 5 are written into a register. Until the counter is written in a subsequent address cycle, this counter counts up in address. This allows block transfer of data into the memories, up to the VME-imposed limit of 256 bytes per block. The addressing sequence involves loading a start address into the register and counter with an address strobe. Subsequent data strobes without an address strobe will increment the counter. A new address strobe will reset the counter to the new value in the data lines. The address goes to the address inputs of the linearization, test and geometric TEC memories. The data that is written into the memories is taken from VME data lines D0-7.

The memories are read in the same manner that they are written. The VME buffer registers are bidirectional to permit data to be placed on the VME data lines. The SETR command is written into the command register and the VME read command is used. The address is set into the register and counter as before and the counter increments with each data strobe unless the address strobe causes a new address to be written. The TEST command enables the writing of test data at the inputs of the linearization, test and geometric TEC memories.

In addition to the memories and command register, there is VME read and write access to the counter for the FIFO that stores data for shipment to the FAST CLEAR and the programmable delays which synchronize each FADC digitization to the incoming pulse. The FIFO is accessed when the address has bits A1-3 = 001, A14=1, and A17-18=11. The card address is set in bits A19-23 as before. The programmable delay is accessed when the address has bits A1-3=010, A14=1, and A17-18=11. The card affected has the address that matches the contents of bits A19-23. The VME address space is summarized in Appendix A.

8. Adder Card: Overview

The Adder Card has 2 principal functions. The first is to continue the process of summing up the energies begun on the TEC. The second is to perform pattern tests on the bits that accompany the energy sums. These pattern tests include counting the number of supertowers

passing each of the energy thresholds, summing up the energy from the threshold test bits in subregions of the region covered by the adder card, and finding isolated muons and electrons.

Every 12 nsec, the pattern logic section of the Adder Card strips off the upper 3 bits and the summing section of the Adder Card strips off the lowest order 9 bits from the 12 bits of data reaching it from each of the 7 TECs it is connected to. The lowest order nine bits are directly injected one of 7 inputs to a 3-stage ECL parallel adder network. These sums are delayed in a FIFO clocked at 24 nsec until the results of the pattern tests are complete so that all results of the Adder Card from one crossing are contained in the same 96-nsec time space, albeit subdivided into 4 words within that time space. This data is shipped to the Trigger Processor as detailed below. The TECs each send a 13th bit to the Adder Card, which toggles between high and low with the transmission of each word every 12 nsec. The Adder Card examines the set of 7 "toggle" bits from each of the 7 TECs connected to it. If any of these bit fails to toggle, the Adder Card sends a trigger error bit to the Trigger Processor Crate. In addition, the history of the previous 16 failures (i.e. which TEC, which cycle, etc.) is kept in a register that can be read via VME commands.

There are two Adder Cards, which are identical in all respects and reside in the middle of the VME crate in positions 11 and 12. One Adder Card is attached to the right and the other to the left half of the split J2 and J3 backplanes. They perform several functions, the first of which is to continue the process of obtaining the total E , E_T , E_x , and E_y . In addition, the Adder Card handles the clock distribution, recognition of isolated Minimum Ionization events, recognition of isolated Electromagnetic events, compares cell energy against preset thresholds, and some simple histogramming (counting) of the individual cell utilization. A control register on each card is written at startup time to indicate which card behaves as the "Master" and which as the "Slave" during certain operations. (These definitions have nothing to do with their VME operation). These operations are described in greater detail below.

As a result of their position in the Trigger crate, the Adder Cards supply the clocking for the Trigger Encoder cards arrayed on either side. The 96 nsec and 12 nsec clocks are ECL differential signals fed from the Trigger Processor crate on a cable reserved solely for the clock. There is separate equal-length cabling from the Trigger Processor crate to each of the Adder Cards. The clocks will be in phase as they enter the Adder Card. All actions in the crate will occur at the time of the rising edge of either the 96 nsec or 12 nsec clock or other clocks generated from these two. A 48 nsec and 24 nsec clock must also be generated for use on the Trigger Encoder card. This will be done on the Adder Card itself. The 96 nsec clock and 12 nsec clock will be distributed on the half J2 backplane as ECL differential signals. These signals will pass through delay lines on the Adder Card set to remove skew between the different clocks as well as to adjust for the different propagation delays between the Adder Cards and the Trigger Encoder cards. The Adder Cards have an 8-bit counter that increments with the receipt of each 96CLK edge. The counter is reset to zero upon receipt of a Crossing 0 Indicator signal. This counter is referred to as the beam-crossing counter and its lowest 4 bits are sent forward to the Trigger Processor.

9. Adder Card: Adder Tree

The adder tree is continued from the TECs onto the Adder Cards. The 9 bit results from each of the Trigger encoder cards is received on a set of lines on the J3 backplane. Each Adder Card handles the data from the seven Trigger Encoder cards plugged into its half backplane. The data is stored in a set of 8-bit registers (100141) as it enters the board. These registers feed four sets of 8 bit adders using 100180's. The overflow bits are ORed together and brought around to be ORed with the adder carry. These four adders combine the data in groups of two from the 63

lines and produce four sums each with 8 bits of dynamic range. The outputs of the adders are fed directly into another set of 100141's. The tree continues with yet another set of 100180's making up two 8 bit adders producing two more results. The dynamic range stays at 8 bits, with subsequent carry's being ORed into a single overflow bit. These two results are also stored in a set of 100141's. Finally, these last two sums are presented to a single 8 bit adder. The result from this last adder is stored in a pair of 100141's.

Up to this point both Adder Cards have been performing the same operations in parallel. The adder cards are identical in that each have the circuitry just described as well as one more stage of addition. Each card feeds its results to another 8 bit adder. It also feeds the same result to a connector at the front of the card. The cable connecting the two adder cards is bidirectional. One of the Adder Cards is designated as the "Master" and the other as the "Slave". This nomenclature is in no way related to Master and Slave as applied to the VME bus. The data from the "Slave" is sent to the other side of the adder on the "Master". The output of the "Slave" is coupled to the input of the "Master". Thus the last Adder on the "Master" combines the data of the two Adder Cards and stores the sum and its carry ORed with the overflow bit in a final pair of 100141's. This last sum is fed out the front of the Adder Card on a cable to the Trigger Processor crate.

10. Adder Card: Subregion Sums

The purpose of the Adder Card subregion sum logic is to compute the energy in subregions of the region of supertowers read in by one pair of Adder Cards. This is done because the region of supertowers covered by one Trigger Crate may not correspond to a region of interest for examination of a specific piece of physics. Such regions of interest include the FCAL supertowers immediately around the beampipe, or an annulus of supertowers 2 or 3 supertowers deep around the beampipe. This should provide a good handle in reducing the beam-gas background. The assignment of supertowers to crates described below covers the FCAL with 4 crates, one per quadrant. The subregion sums are used by the Trigger Processor to calculate the energy in rings of FCAL supertowers around the beampipe by summing the appropriate subregion energies from each of the 4 FCAL Trigger Crates. These same subregions are also used to calculate the symmetry of energy deposited around the beampipe.

The energy deposition from beam-gas interactions is expected to be more symmetric than ep interactions. The energy in the boundary regions between FCAL and BCAL or BCAL and RCAL is expected to cause difficulties in triggering. A sum of energy in these regions will enable the Trigger Processor to modify requirements for events depositing energy there. The full definition of subregions over the calorimeter is described in the section on Assignment of Trigger Crates and Supertowers. The subregion logic sums up the energy in 8 independent subregions, as well as computing a full 56-supertower region sum from the threshold test bits. While this uses the coarse 3-bit scale of the threshold bits, the subregions are fully programmable because the assignment of a supertower to any one of the 8 regions is made through a downloaded table.

The Adder Card subregion sum and threshold sum logic uses the lower 3 bits of the data coming from each of the 7 Trigger Encoder Cards to which it is connected. Each Trigger Encoder Card sends 24 bits of information in 8 3-bit words that arrive once every 12 nsec, as shown in Table 4. The Trigger Encoder Cards cover 4 supertowers apiece, each of which contributes the 6 bits of test information delineated in the section on the Trigger Encoder Card tests. The first three bits (QU, MI, and EM) are used by the pattern logic and the second three bits (T1, T2, and T3) are used to compute the energy sums in subregions and total number of supertowers exceeding each threshold. The information on the first supertower is complete after 24 nsec, the second after 48 nsec, the third after 72 nsec and the fourth after 96 nsec. The QU, MI, and EM bits arrive

on every odd 12 nsec cycle and the T1, T2 and T3 bits arrive on every even 12 nsec cycle. The Adder Card operates on this information as it arrives during the 96 nsec time span, shifting it forward to the pattern logic and energy sum ECL 8-bit registers (100141's). After 96 nsec, each Adder Card has received information from 28 supertowers. The two Adder Cards combine their information to search for patterns, make subregion sums and count thresholds exceeded in a 56-supertower region.

The Adder Card calculates the energy in 8 non-overlapping subregions of the 56-supertower region by computing the energy from the threshold test information. These subregions are programmable and may be completely remapped under software control. One set of subregions is shown in Figure 9. The numbering of supertowers in Figure 9 is only used for description of the circuits. The actual supertower numbering is described in a subsequent section. The 56 supertowers are assigned to either the contained subregion (30 supertowers) or the edge subregion (26 supertowers). The number of thresholds exceeded in each of these subregions is then used to calculate a contained energy and an edge energy. These subregions are further subdivided into groups of supertowers that are close to the beam-pipe which represent a beam-gas subregion, and the other supertowers into a non-beam-gas subregion. A third set of four subregions is made to include those supertowers on each of the four edges of the 56-supertower region. The corner supertowers may be assigned to either edge they adjoin. Another regional division may be made in order to match calorimeter subregions with the regions of the Central Tracking Detector (CTD). The geometry of the subregions is further described in the section on assignment of Trigger Crates and Supertowers.

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56

E	E	E	E	E	E	E	E
E	C	C	C	C	C	C	E
E	C	C	C	C	C	C	E
E	C	C	C	C	C	C	E
E	C	C	C	C	C	C	E
E	C	C	C	C	C	C	E
E	E	E	E	E	E	E	E

Figure 9. Assignment of supertowers in a 56 supertower region as either "edge" (E), or "contained" (C). The numbering is used only for the circuit description.

The two Adder Cards together are able to sum the energy in up to 8 different subregions of the 56 supertowers. These sums are performed on the data coming into each Adder Card without consideration of the data being received by its partner. The Adder Cards make these sums independently. The two Adder Cards send partial sums to each other and perform the final summation to make up the entire subregion. This mode of operation permits the creation of a single design for the Adder Card. The only difference between the two cards is the designation of one of them as the Master and the other as the Slave. This is done by software command and the principal distinction between the two is which data each sends to the other.

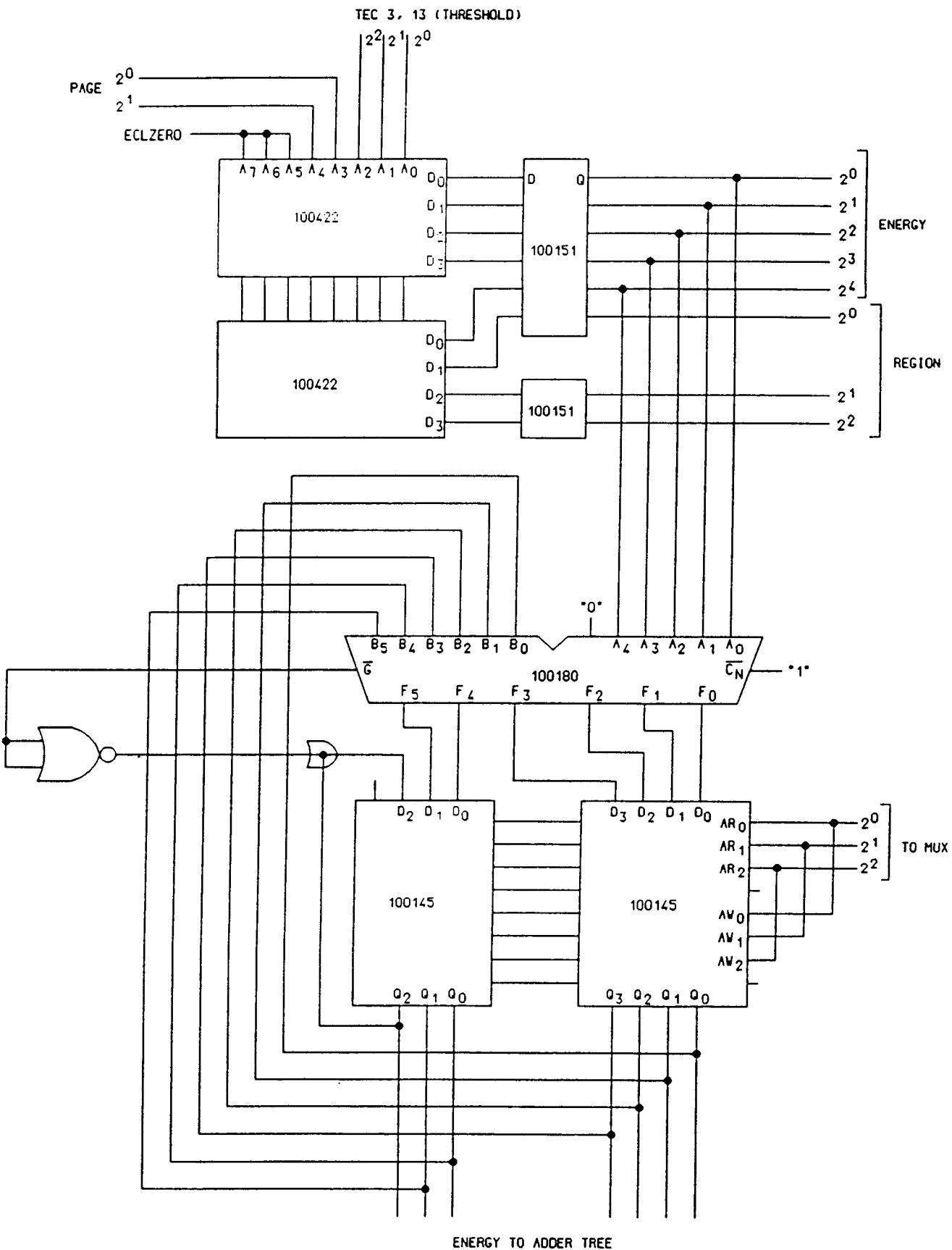


Figure 10. Adder Card Subregion Energy Sum Logic.

One of the seven sections of threshold energy sum logic is shown in Figure 10. Each 3 bit threshold test is passed forward to a lookup table constructed from a pair of 256X4 ECL RAM's connected as a single 256X8 bit memory. The address of the RAM is formed from the 3 bits of threshold information plus 2 bits to indicate which of the four thresholds is under examination. The output data from the RAM is divided into two words. The first is five bits long and represents the energy associated with the threshold present on the Address lines. The second is 3 bits and indicates which subregion contains this particular threshold.

Seven memories work in parallel each handling four words of threshold information from one of the seven TEC cards connected to the Adder Card. The data from the memories is fed forward to 7 ECL 8-bit registers (100141's). This bank of registers is used to hold the data for accumulators that follow. Each accumulator is made up of an adder section followed by a memory section. The adder section uses a six bit ECL parallel adder (100180) with carry in and carry out. The memory section uses a pair of registers (100145's) with separate read and write addresses and an output latch that can retain the last data read. The memory can also be cleared via a single reset line.

The accumulator operates on two 12-nsec cycles. The first cycle is a read. The three bits of subregion information are supplied to the read address to access the location in the memory associated with a particular subregion. The data is held in the output latch and presented to one side of the adder during the second cycle. The other side of the adder is fed by the 5 bits of energy from the lookup table. The sum of this energy, with the value that had been in the accumulator, is stored back into the same location of the accumulator. At the end of four 24-nsec cycles the accumulator has non-zero values in at least one location and at most four. Since the specific non-zero locations are not determined, all eight locations are read out.

The seven memories are read at the same time and fed into a three level adder tree. Since new data is entering at the same time the accumulators are being emptied of their information, it is necessary to double buffer the data. Two set of accumulators are required. One accumulator is used during one 96 nsec cycle while the other is being read out, and then during the second 96 nsec clock cycle the other is used while the first is read out.

The outputs from the double set of accumulators are connected to quad 2:1 Multiplexers (100155's). The select input is wired to a signal (SELECTR) that goes through one complete cycle every 192 nsec. The outputs of the multiplexers feed a three stage adder tree made up of six bit parallel adders (100180's) and registers (100141's) between stages of adders. The data enters the adder tree 7 bits wide and leaves it 8 bits wide. Stages two and three of the adder tree have single bit right shifts hardwired in to force the data into an eight bit range. The last stage of the adder tree is then fed to a final eight bit adder to combine the data from the adder tree with the data from the adder tree of the Slave Adder Card. This result is stored in a set of registers.

The outputs of the registers are connected to the data inputs of a pair of additional registers clocked on alternate phases of the 12-nsec clock, followed by a further pair of registers clocked out by the 24-nsec clock to a quad driver (100113) that sends the data (50 Ω differential) over the output cable to the Trigger Processor Crate. In addition to the 8 subregion sums, the total energy in the 56-supertower region is also computed from the threshold tests. This is accomplished by building an accumulator out of adders (100180's) and registers (100141's). The outputs of the registers in the accumulator are connected to one side of the accumulator adders. The other side of the accumulator adders is fed by the last register in the adder sum tree discussed above. This accumulator structure is used to compute the energy. This total energy and the 8 subregion sums are sent forward to the Trigger Processor Crate as one 10-bit and 8 8-bit numbers respectively.

11. Adder Card: Threshold Sums

The Adder Card sums up the number of supertowers in the 56-supertower region exceeding each threshold and not the one above it. It sums up supertowers passing no threshold and those with overflows. The purpose of this logic is to search for jet candidates. If a region has a uniform deposition of energy than no supertowers will pass the higher thresholds and this indicates a lack of jets. If the energy deposition is peaked around a few supertowers, then it is likely that there is a jet and there will be supertowers passing the higher thresholds. Therefore, a jet likelihood may be inferred from the number of supertowers passing the various thresholds and setting these bits. More importantly, the jet-finding algorithms used by the higher level triggers involve the selection of seed towers -- towers with high energy. If there are no supertowers passing the higher energy thresholds, then there are no jets to be found. The Trigger Processor counts the number of supertowers exceeding thresholds both regionally and globally to create a jet likelihood.

The threshold sum logic is shown in Figure 11. The 3 threshold test bits are passed forward from the input ECL registers (100141) to two multiplexers (100155) that switch between sending out right and left sets of three bits. The bits of threshold information are simultaneously passed to the left three bits of the first multiplexer and the right three bits of the second multiplexer.

The three bits of pattern information are produced by a three-bit cycling counter that sends the sequences 000 through 111. These patterns correspond to passage of no threshold, the first threshold, etc. as described in the test description of the Trigger Encoder Card. These patterns are simultaneously sent to the right three bits of the first multiplexer and the left three bits of the second multiplexer. Both multiplexers are driven by a select line that selects the right three bits (SELECTR). The SELECTR line toggles from high to low by each 96 nsec clock edge.

Each of the multiplexers has its three data lines and its input select bit connected to a 4 word \times 4-bit Content Addressable Memory (100142). One of the Content Addressable Memories (CAM's) has 4 3-bit Threshold Test words (3 bits from each of 4 supertowers as described in Table 4) read in on its data lines and written by a write pulse at the rate of one word every 24 nsec. The four address lines are connected to a 4-bit shift register with a single 1 in it shifting with the 24 nsec clock. This causes each of input words 1 through 4 to be written into addresses 1 through 4. The other CAM has the 8 possible patterns compared with the 4 data words read in during the previous 96 nsec at the rate of 1 pattern every 12 nsec. Each of the four threshold words that matches the input pattern raises its output line. If all four patterns match, then all four output lines are high. In one 96 nsec time period, the output of the CAM is a sequence of 8 4-bit numbers indicating which of the supertowers exceeded each threshold, but not the threshold above. Each of the two CAM's assigned to the 4 supertowers provides these 4 bits as an address to half of a 256 \times 4 memory. The other 4 address bits of this memory are provided by one of the two CAM's assigned to a neighboring group of 4 supertowers. This memory serves as a lookup table that produces a 4-bit sum of the 8 individual input bits. Since at least none and at most 8 supertowers can exceed a particular threshold, 4 bits are necessary to count the number of supertowers. The output lines of the pairs of 256 \times 4 memories used by two 4-supertower groups are bussed together and each memory sends out its data under control of SELECTR, alternating every 96 nsec.

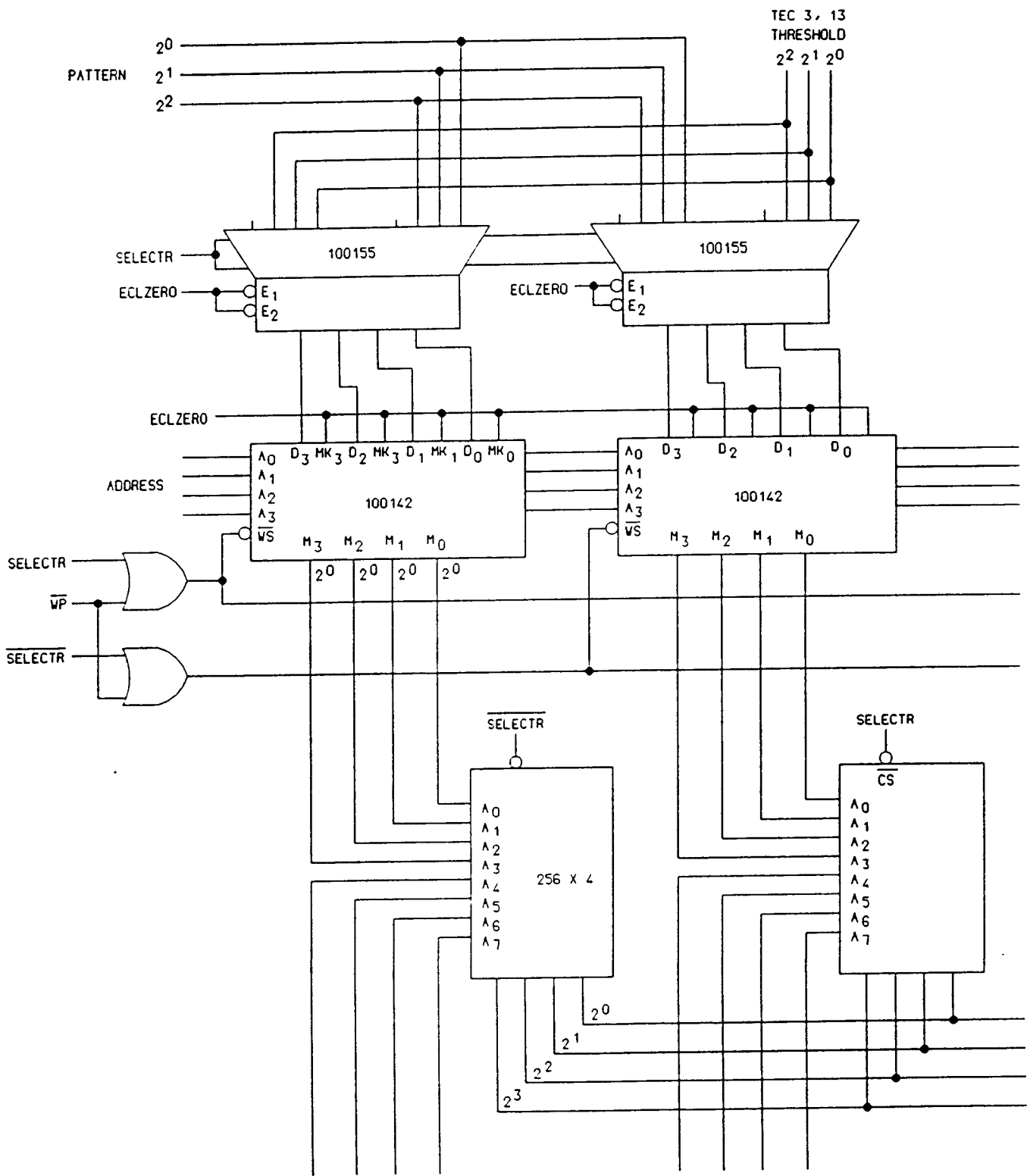


Figure 11. Adder Card Threshold Sum Logic.

The 7 groups of 4 supertowers are serviced by 7 pairs of multiplexed CAM's connected to 4 256X4 that feed 4 bit numbers to a two stage adder tree clocked at 12 nsec. The adder tree is composed of ECL parallel adders and registers. It produces a 6-bit result in 24 nsec, which is presented as an address to a two 1KX4 memories organized as a single 512X6, where the 9 bits of address include the 6-bit adder tree result and 3 bits of page. The 8 pages cycle at a 12 nsec rate to match the results on each of 8 threshold sums emerging from the adder tree. Page 0 of this memory is a 6-bit word counting the number of supertowers passing no threshold. Pages 1 and 2 contain 5-bit words counting the number of supertowers that passed the first threshold (but not the second) and the second threshold (but not the third), respectively. Pages 3 through 6 have 4-bit words counting the number of supertowers that passed the third threshold (but not the fourth), fourth threshold (but not the fifth), the fifth threshold (but not the sixth), and the sixth threshold (but not an overflow), respectively. Page 7 contains a 3-bit word counting the number of overflow supertowers. All of these words are set to the maximum value if their range is exceeded.

12. Adder Card: Pattern Logic

The purpose of the Adder Card pattern logic is to identify isolated muons and electrons. This task is complicated by the edges of regions covered by different Trigger Crates, where isolation requires information from two or more crates. This difficulty is surmounted by counting the number of isolated electrons and muons separately for those in the contained part of the region and on each of the four edges. The corner supertowers are assigned to one of the adjoining edges for these purposes under programmable control. The definition and numbering of the region edges is described in the section on assignment of Trigger Crates and Supertowers.

The identification of isolated electrons is important because it permits triggering without a Q^2 cut. Since the rate of isolated electron production is low, if the identification does not trigger at too high a rate from isolated hadrons, each isolated electron constitutes a good trigger. The isolation requirement is necessary to prevent a high background rate from hadrons and should not veto many legitimate neutral current events. The pattern logic first tries to establish an electromagnetic signal in a central region of either 1,2,3, or 4 towers, and then checks that the surrounding (up to 12) supertowers are quiet.

The logic to identify the isolated muons is the same as that used for the isolated electrons except, where one uses the EM bits, the other uses the MI bits. The identification of muons has always been important to triggering, because it is a signal of heavy quark, neutral heavy lepton, or gauge boson production. While the Zeus detector has muon systems, they do not cover all of the calorimeter area. In addition, the muon systems may not be able to exactly identify the crossing that triggered the event, whereas all calorimeter triggers are tied to a single crossing. The existence of a good calorimeter muon trigger also is useful for calibration purposes, since it indicates a minimum ionizing particle with a trajectory traversing a single supertower.

The pattern logic of the Adder Card uses the upper 3 bits of the data coming from each of the 7 Trigger Encoder Cards to which it is connected. The pattern logic searches for a single or group of up to 4 supertowers with electromagnetic or minimum ionizing test bits set that are completely surrounded by "quiet" supertowers. These are counted as contained isolated electrons or contained isolated muons. The pattern logic also searches for groups of supertowers that satisfy these conditions, but have one or more electromagnetic or minimum ionizing supertowers next to the 56-supertower region boundary. In these cases, isolation on one of the sides cannot be proved without checking the adjacent 56-supertower region. These are counted as edge isolated electrons or edge isolated muons. The total number of edge isolated muons and electrons are counted for each of the four edges. Examples of edge and contained isolated muon patterns are

shown in Figure 12. The pattern logic also flags which of the four individual edges are "quiet", i.e. have Q, M, or E bits on in every supertower. This information is used by the Trigger Processor in verification of edge isolated electrons and muons.

X	X	X	X	X	X	X	X
X	Q	Q	Q	X	X	X	X
X	Q	M	Q	X	X	X	X
X	Q	Q	Q	X	Q	Q	Q
X	X	X	X	X	Q	M	Q
X	X	X	X	X	Q	M	Q
X	X	X	X	X	Q	Q	Q

X	X	X	X	X	X	X	X
Q	Q	X	X	X	X	X	X
M	Q	X	X	X	X	X	X
Q	Q	X	X	X	X	X	X
X	X	X	X	X	X	X	X
X	X	Q	Q	Q	Q	X	X
X	X	Q	M	M	Q	X	X

Figure 12. Examples of two patterns accepted as contained isolated muons (left figure) and two patterns accepted as edge isolated muons (right figure). supertowers are labelled as quiet (Q), minimum ionizing (M), or do not care (X). The same patterns satisfy the isolated electron test if the same supertowers passing the minimum ionizing test, would pass the electromagnetic test instead.

The Isolated Minimum Ionization test will be performed on the Master Adder Card and the Isolated Electromagnetic test will be performed on the Slave. The Q, M, and E test results come to the card three bits wide on the same backplane lines as those results of the energy threshold tests. The values from all eight cards in parallel are stored in a set of 3 registers (100141's), distinct from those mentioned above, for the energy threshold tests. A cable bridging the two cards carries the appropriate information from one card to the other. Seven pairs of bits must be transmitted in either direction every 24 nsec. One bi-directional cable will be used between identical connectors on the two cards. The Master will send its data first -- eight bits of Q and eight bits of E. On the next 12 nsec cycle the Slave will have control of the cable and will send its seven bits of Q and seven bits of M. The Master/Slave bit in the control register will define the proper timing and selection of bits for each card. The data is received and stored in a separate set of registers on each of the Adder Cards.

The type of isolated supertower to be identified is slightly different depending on whether the supertower occurs in the edge or contained subregion of the 56-supertower region. The implementation of the hardware for the contained subregion is discussed first since it requires more generality than that used for the edge subregion. The procedure described below finds isolated muons in the contained subregion. The identical procedure is followed to find isolated electrons, with the requirement of a minimum ionizing bit replaced by an electromagnetic bit.

On the Master Adder Card the 56 Quiet (Q) and 56 Minimum Ionizing (M) bits are each read out of the input registers or the cable from the Slave Adder Card into 7 Q and 7 M 8-bit ECL shift registers (100141). On the Slave Adder Card, the Q and Electromagnetic (E) bits are read into the same series of shift registers. The pairs of bits (Q and M or Q and E) in the 8 x 7 supertower region is read into and out from these 7 pairs of shift registers in 8 12-nsec steps. These shift registers are read out from the side into 7 sections of logic that look at a slice of the 8

*	*	*	*
*	Q	Q	*
*	Q	Q	*
*	*	*	*

Fails Test.
 Q = Quiet
 M = Min Ion
 X = Don't Care
 * = Don't Check

Q	*	*	X
*	M	Q	*
*	Q	Q	*
*	*	*	*

PATTERN 0

*	*	*	*
*	Q	M	*
*	Q	Q	*
*	*	*	*

Selected by
 Logic of
 Right Neighbor.

Q	*	*	Q
*	M	M	*
*	Q	Q	*
*	*	*	*

PATTERN 1

*	*	*	*
*	Q	M	*
*	Q	M	*
*	*	*	*

Selected by
 Logic of
 Right Neighbor.

Q	*	*	X
*	M	Q	*
*	M	Q	*
*	*	*	*

PATTERN 2

*	*	*	*
*	Q	Q	*
*	Q	M	*
*	*	*	*

Selected by
 Logic of
 Right Neighbor
 Next Cycle

Q	*	*	Q
*	M	M	*
*	M	Q	*
*	*	*	*

PATTERN 3

Figure 14. Classification of Patterns made by the first 1Kx4 memory in the Adder Card Pattern Logic.

X	*	*	Q
*	Q	M	*
*	M	Q	*
*	*	*	*

PATTERN 3

M = Min Ion
 Q = Quiet
 X = Don't Care
 * = Don't Check

Q	*	*	X
*	M	Q	*
*	M	M	*
*	*	*	*

PATTERN 5

Q	*	*	Q
*	M	M	*
*	Q	M	*
*	*	*	*

PATTERN 4

X	*	*	Q
*	Q	M	*
*	M	M	*
*	*	*	*

PATTERN 5

Q	*	*	X
*	M	Q	*
*	Q	M	*
*	*	*	*

PATTERN 4

*	*	*	*
*	Q	Q	*
*	M	Q	*
*	*	*	*

Selected by next cycle, unless last cycle (bottom edge) then **PATTERN 6**

Q	*	*	Q
*	M	M	*
*	M	M	*
*	*	*	*

PATTERN 5

*	*	*	*
*	Q	Q	*
*	M	M	*
*	*	*	*

Selected by next cycle, unless last cycle (bottom edge) then **PATTERN 7**

Figure 14. (cont'd) Classification of Patterns made by the first 1KX4 memory in the Adder Card Pattern Logic.

The first stage of pattern classification is illustrated for a 16-supertower region in Figure 14. When all four central supertowers are quiet, the region tested cannot have an isolated muon. Since all of the 16-supertower patterns overlap, there are patterns that can be pass the tests in two adjacent overlapping search regions. In order to avoid double-counting, the patterns that can be picked by two search regions are selected by the right hand search region only. Similarly, there are patterns that pass in a particular supertower search region and would pass again when the pattern moves down one step. Such patterns are be selected by one of the 8 parallel logic circuits, but they pass during two of the 12 nsec cycles of the same circuit. In order to avoid double-counting, the patterns are selected by the bottom, or last search region that they pass. Patterns 6 and 7 in Figure 14 illustrate these patterns.

If the search pattern that would usually allow selection by the right neighbor logic or the next cycle is located on the right or bottom edge, the pattern is then selected as an edge pattern. There are 6 classes of patterns illustrated in Figure 14 that are selected whether they are edge or contained patterns.

Once the first classification of patterns 0 through 7 has been made, this information is forwarded to the second half of the logic for confirmation that the appropriate combination of quiet supertowers necessary for each classification to be identified as an isolated muon is present. Since the central four supertowers, and upper corner supertowers have been already checked, only the remaining supertowers on the edge of the 16-supertower region need to be examined.

The process of examination is illustrated in Figure 15. Referring once again to the example of the contained search region shown in Figure 13, supertowers 9, 12, 18, 19, 26, and 27 are examined in the first stage of the logic and supertowers 10, 11, 17, 20, 25, 28, 33, 34, 35, and 36 are examined in the second. All of the patterns with the exception of the bottom edge patterns 6 and 7 require supertowers 10, 11, 17, and 25 to be Q. This is checked by requiring an AND of these bits in all cases except a bottom edge. The remaining supertowers, 20, 28, 33, 34, 35, and 36, are fed to a lookup table for the pattern testing shown in Figure 15. The lookup table has the three bits of the first stage classification along with the a bit indicating Q or not Q for the supertowers occupying positions corresponding to supertowers 20, 28, 33, 34, 35 and 36. One additional bit indicating whether the supertower search region is on a bottom edge takes care of the special cases for patterns 6 and 7.

The pattern logic circuitry is illustrated in Figure 16. There are 8 parallel sections of logic such as this on each Adder Card. The Q and M bits are clocked into an 8-bit register (100141) and presented to the first of the two 1Kx4 memories (SSM100474-8) every 12 nsec. Figure 12 shows the specific cycle of the logic that examines the supertower search region shown in Figure 13. The particular logic that performs the search for the Figure 13 region is the second set of 8 such set of logic and hence its signals are labelled 1 (since the first set is labelled 0). The address presented to the memory during this cycle includes the Q bits for supertowers 9, 12, 18, 19, 26 and 27, and the M bits (or E bits for the logic on the Slave Adder Card) for supertowers 18, 19, 26, and 27. The contents of the memory include three bits for the patterns classified as shown in Figure 14. The fourth bit indicates a failure to find any pattern.

The four bits of memory contents are presented to a register (100151) which is then connected to a second memory lookup table. This is another 1Kx4 memory (SSM100474-8) that is clocked at 12 nsec. The pattern failure bit from the first memory is connected to the disable on the second. If this bit is set, the memory presents 0 on its data lines. The three bits of pattern classification become the first three bits of address for the memory. Since the tests involving the supertower search region shown in Figure 13 occur in the second memory 12 nsec after the tests done in the first memory, at the time that the first memory is testing the supertowers in the search region, the lines that will carry the these same supertowers to the second memory have the

previous group of supertowers on them. As specified above this memory has to test on Q bits, passing through the shift register, for supertowers 20, 28, 33, 34, 35, and 36. At the previous 12 nsec cycle, the lines that will carry these bits carry the Q bits for supertowers 12, 20, 25, 26, 27, and 28. These form address bits 3 through 8. Address bit 9 is a bit indicating that the bottom edge supertower bits entered the first memory on the previous cycle. The bit is therefore entitled "LAST", but delayed one 12 nsec cycle so it is in time with the arrival of the bits at the second memory, hence it is called "LASTD".

Three bits of the memory contents are read from the second memory. The first indicates a contained isolated muon (CONTND). The second bit indicates that the pattern is on the bottom edge (BEDGE). If LASTD is true, BEDGE is set for patterns 2 through 7 of Figure 15, without a check on the bottom row of supertowers. (Patterns 0 and 1 are contained and not bottom edge regardless of the state of the supertowers on the bottom row). The third bit indicates that the central part of the pattern is on the bottom edge (LOWBOT). This bit is used to eliminate the top center two supertowers from the Q requirement since they do not need to be checked to verify isolation. If LASTD is true, LOWBOT is set for patterns 6 and 7 only of Figure 14. On the next 12 nsec cycle, the top center supertowers are checked (unless a LOWBOT). For the example of the search subregion shown in Figure 12, these are supertowers 10 and 11. Since the Q bits for these supertowers are combined together simultaneously with the tests performed by the second lookup memory, the lines carry supertowers 2 and 3 when the first memory is performing the pattern tests on the Figure 13 supertower search subregion. After the lines carrying the Q bits for supertowers 2 and 3 are combined, the result is combined with LOWBOT to form the quiet top signal, TOPQ, and presented with BEDGE and CONTND as three bits into a register (100151).

A contained isolated muon (CONTAIN) is derived from the AND of the CONTND and TOPQ lines with the quiet bits from the left edge center supertowers. For the contained search subregion in Figure 13, these are supertowers 17 and 25. Since this operation happens two 12-nsec cycles after the test for the Figure 13 contained search subregion is performed in the first memory, the lines that will carry Q bits for supertowers 17 and 25, carry Q bits for supertowers 1 and 9 at the time of the first memory test.

The final input to the contained muon AND is a bit indicating that the supertower search subregion is not on the top edge. If the search subregion is at the top edge, then the muon is an edge isolated muon and should not be counted as contained. The bit which indicates that the supertower search is the first to be performed by the first memory for a particular crossing is delayed by two 12-nsec cycles and input to the AND as "FIRSTDD" (each D stands for one 12-nsec cycle of delay).

A bottom edge isolated muon (BOTEDGE) is derived from the AND of the TOPQ and BEDGE bits with the Q bits from the left edge center supertowers. A top edge isolated muon (TEDGE) is derived from the AND of the CONTND and FIRSTDD bits with the Q bits from the right edge center supertowers.

*	Q	Q	*
Q	M	Q	X
		0	
Q	Q	Q	X
X	X	X	X

Q = Quiet
M = Min Ion
X = Don't Care
* = Already Checked

*	Q	Q	*
Q	M	Y	Q
		4	
Q	Q	M	Q
X	Q	Q	Q

*	Q	Q	*
Q	M	M	Q
		1	
Q	Q	Q	Q
X	X	X	X

*	Q	Q	*
Q	Y	Y	Q
		5	
Q	M	M	Q
Q	Q	Q	Q

(At least of Y's must be M)

*	Q	Q	*
Q	M	Q	X
		2	
Q	M	Q	X
Q	Q	Q	X

*	*	*	*
Q	Q	Q	*
		6	
Q	M	Q	*

BOTTOM EDGE

*	Q	Q	*
Q	Y	M	Q
		3	
Q	M	Q	Q
Q	Q	Q	X

Y = M or Q.

*	*	*	*
Q	Q	Q	Q
		7	
Q	M	M	Q

BOTTOM EDGE

Figure 15. Completion of Isolation Verification of Patterns made by the second 1KX4 memory and subsequent Pattern Logic in the Adder Card. Note that the Top and Left Edge Q's are required for all patterns except those on the bottom edge.

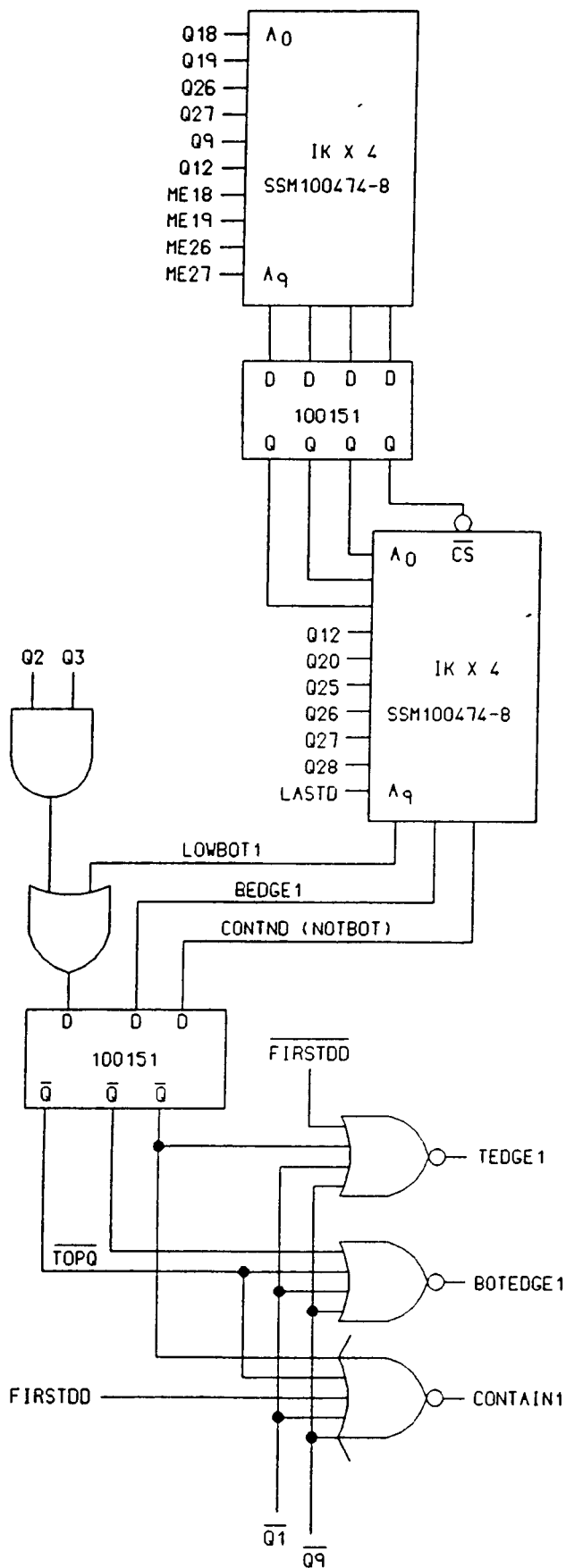


Figure 16. Adder Card Pattern Logic.

The logic also locates left and right edge isolated muons (M's). The slice used to handle the left hand edge is identical to those used to locate the isolated M's in the contained subregion of the 56-supertower region. The only difference is the manner in which the logic is wired to the Q and M inputs of the memories as presented by the shift register. The sliding 4 x 4 subregion used to perform the pattern test is now one over to the left of the subregion used to illustrate the previous example. Figures 9 and 13 show that if the 4 x 4 subregion is moved over one column to the left the left-most column will extend beyond the edge of the 56-supertower region. The values in this column are assumed to be Q's. In this slice none of the patterns in the first 1Kx4 memory can be contained M's. Therefore the possible pattern classifications are top edge, left edge, and bottom edge. In the case in which a pattern is in the top or bottom corner it is determined to be both top and left edge or bottom and left edge, respectively.

The output of the first memory encodes each of the eight possible patterns in the same manner as that used in the contained example. The fourth bit is still an indication that one of the eight valid patterns has been detected. If set, this bit disables the outputs of the second memory. These four bits are stored in an intermediate register to be presented to the second memory in the next 12 nsec cycle. The second memory is wired to take into account the fact the 4 x 4 subregion is shifted to the left in the 56-supertower region. Since there can be no contained M's in this slice, the outputs from the the second memory are redefined. LOWBOT and BEDGE are the same, but CONTND is changed to LEDGE. As before, LOWBOT is true when LASTD is true and patterns 6 or 7 have been detected. BEDGE is true when LASTD is true and any one of patterns 2 through 7 have been detected. LEDGE (left edge) is true for all valid patterns. These patterns, along with the logical AND of the Q bits from supertowers 9 and 10 are stored in a register and will be processed in the next 12 nsec cycle.

The left edge slice logic does not need to perform the AND of the Q's for the supertowers to the left of supertowers 17 and 25. These supertowers are off the left hand edge of the 56-supertower region and are assumed to be quiet. The outputs of the register (100151) following the second memory are decoded directly to give LEDGE (left edge), BOTEDGE (bottom edge), and TEDGE (top edge). Top edge occurs for any valid pattern detected during the first cycle.

The right edge is handled in a similar fashion. However, two slices are used to detect right hand edge isolated M's. The first has its 4 x 4 search subregion overlapping the 56-supertower region with the right-most column extended just past the right hand edge of the 56-supertower region. The second is extended two columns past the right hand edge of the 56-supertower region. Figures 9 and 13 illustrate the position of the search subregion.

The first memory is wired as in the previous two examples., However the data for the supertower to the right of supertower 16 is not available and is assumed to be quiet. The corresponding input to the first RAM is wired TRUE. The valid patterns are the same as before. The fourth bit is used to enable the outputs from the second memory. The second memory is connected in a similar fashion. In this case the data for supertowers to the right of supertowers 16, 24, and 32 are unknown and assumed to be quiet. For this particular case all four of the memory's output bits are defined. The first two, LOWBOT and BEDGE, have the same definitions given above. The third, CONTND, is true for patterns 0 and 2. The fourth, REDGE, is true for patterns 1, 3, 4, and 5. It is also true for pattern 7 if LASTD is true. These four bits are stored in a register and are encoded in the next 12 nsec cycle to provide the edge and contained information. The Q bits from supertowers 15 and 16 are also combined in this cycle and the result stored in the same register with the four bits from the memory.

Four results are generated in the next 12 nsec period: TEDGE (top edge), BOTEDGE (bottom edge), CONTAIN (contained), and RTEDGE (right edge). The quiet bits from supertowers 22 and 30 must always be true for any of the valid patterns (see right edge

supertower search region in Figure 13). TEDGE is true only during the first cycle. It requires the logical OR of CONTND and REDGE which are in turn enabled by the quiet bits of supertowers 15, 16, 22, and 30. BOTEDGE is only true during the last cycle and is essentially BEDGE enabled by the same four supertowers. CONTAIN is fairly restrictive in this slice. It is the result of CONTND enabled by NOT FIRSTDD and the quiet bits from the four supertowers. Finally, RTEDGE is just REDGE enabled by the same quiet bits.

There are a few special cases of right edge isolated M's that are handled by an additional logic slice running in parallel with the other 7 logic slices. This slice handles a 4 x 4 subregion placed one column to the right of the right edge subregion in Figure 13. Since half the pattern is over the boundary of the 56-supertower region, the data from eight of the supertowers is unknown and assumed to be quiet. The wiring to the first memory is similar to that of previous examples except that the Q and M bits from the supertowers to the right of the 56-supertower region are wired true. Only patterns 0, 2, and 6 will be fed forward to the next memory.

The second memory also has a number of its address bits wired true. The appropriate quiet bits are brought in for this 4 x 4 subregion as well as LASTD. Only three bits of information are read out from this memory. They are LOWBOT, BEDGE, and REDGE. The definitions for LOWBOT and BEDGE are the same as in the previous examples. All valid patterns force REDGE TRUE. These three bits are stored in an intermediate register for proper encoding in the next 12 nsec cycle.

The final results from this slice are REDGE, BOTEDGE, and TEDGE. They have the same definitions as those from the right edge slice discussed. TEDGE is only valid during the first cycle. REDGE and BOTEDGE are enabled by the AND of the three supertowers at positions 16, 23, and 31. There is no fourth supertower included in this AND since it is past the boundary of the 56-supertower region.

Each 12 nsec cycle generates information on the number of contained and isolated M's in a portion of the 56 supertower region. It takes 7 cycles to produce a count of the total number of contained, top edge, bottom edge, left edge, and right edge isolated M's. During each cycle six bits (CONTAIN1 - CONTAIN6) are generated in parallel. These bits are presented to the address inputs of a 1KX4 RAM. A lookup table in the RAM combines the bits and produces a binary coded output representing the total number of CONTAIN bits found for that cycle. This number is stored in a register that immediately follows the RAM. The output of the register is fed back into three more of the address bits of the same RAM. On the next cycle the lookup table in the RAM will combine these binary coded bits with the CONTAIN bits to generate a new binary coded number. The number of contained M's is limited to 7. The lookup table in the RAM is designed so that once the count has reached 7 it will stay at 7. The remaining address bit on the RAM is wired to FIRSTDD. This signal is used to force the outputs of the RAM to 0, thus effectively clearing the count to zero. The total number of contained M's is available after seven 12 nsec cycles.

Each 12 nsec cycle generates only one bit of left edge isolated M's. This bit is used to enable the incrementing of a four bit counter, with the output giving a maximum of 3. Only two bits are used to record the number of isolated left edge M's.

Top edge information is available only during the first cycle. It is produced by all the slices in the pattern search logic. Therefore eight bits are generated in parallel in one 12-nsec cycle. These are presented to a 256X4 RAM containing a lookup table that effectively forms the binary encoded number of the sum of the individual bits. This number is not allowed to overflow 2 bits. It is stored in a register until all the other edge information is available.

Bottom edge information is available only during the last cycle. As with the top edge a single bit is produced from any one of the eight slices. These bits are fed into the same RAM as

used by the top edge bits. The result is kept within a two bit range. The result is stored in a register until the rest of the pattern information is available.

Right edge information is made available from the last two slices during any one of the 7 cycles. An OR is made from the right edge bits of the last two slices and the result fed into the enable of a four bit counter. This counter is treated in the same manner as that used for the left edge information. The result is limited to two bits and held until the rest of the pattern information is available.

The two bits from each of the edge counts are fed into the address inputs of another 256X4 RAM. The lookup table contained in this RAM is used to combine each of the two-bit binary encoded fields into a single three-bit count. This count is not allowed to overflow. The results are held in a register until all the results from the pattern searching and threshold summing are available.

13. Trigger Crate: Bus and Card Structure

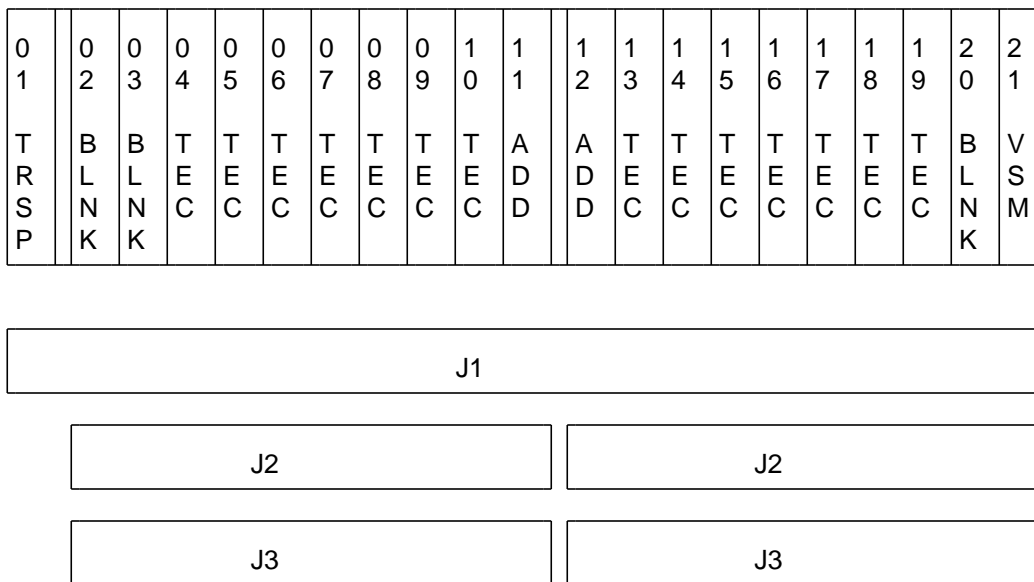


Figure 17. Assignment of modules to slots in trigger VME crates with backplane divisions shown below. Trigger Encoder cards are labelled TEC, Adder Cards are labelled ADD, the VME Service Module is labelled VSM, blank slots are labelled BLNK, and the Nikhef 2-Transputer board is labelled TRSP. The J1 bus is connected to all 21 slots. The J2 and J3 busses are broken between slots 11 and 12 and do not continue to slot 1. All user-defined lines on the continuous sections of the J2 and J3 busses are linked together. The J2 connector for the 2-Transputer board (slot 1) is used to bring out the Transputer Links.

The Trigger Crate contains two groups of 7 TECs connected to a single Adder Card. The TECs communicate with the Adder Card over the J2 and J3 backplanes. The J2 and J3 backplanes have all lines bussed together and are split between the 2 adder cards as is shown in Figure 17. In this sense, the J2 and J3 backplanes are non-standard since they have all the lines connected to each other with the exception of a break between slots 11 and 12. In addition, these backplanes do not extend into the first slot, where the Nikhef 2-Transputer board is located. This is because this board brings the transputer links out over the user-defined pins on the J2 backplane. The crate also has a VME service module in the 21st slot. This module contains an

IEEE interface used for voltage monitoring. The J1 backplane is operated in the standard manner, yielding 24 address lines and 16 data lines. The assignment of these lines is detailed in Appendix A.

The TECs use 12 lines each on the J3 and J2 backplanes to send their data via 12 nsec ECL transmission to the Adder Cards. In addition, there is one line for each TEC that toggles from high to low every 12 nsec with the sending of each new word on the 12 data lines. The Adder Card uses these 7 lines to verify that the TECs are sending data. The Adder Cards send out 96 nsec and 12 nsec clock signals to the TECs on these backplanes as well.

14. Assignment of Trigger Crates and Supertowers

Each Trigger Crate services a group of 7 x 8 supertowers. The organization of Trigger Crates 0 - 3 in the FCAL EMC section is shown in Figure 18. These EMC sections are projected into the HAC's to form the trigger supertowers. The mapping of the FCAL EMC towers into groups of 7 x 8 supertowers requires the summing of separate EMC towers into single towers as shown. In addition, three HAC0 towers are also read in along with the other 53 groups of 4 EMC towers. The projection of the BCAL EMC sections into the FCAL is shown. Since the HAC0 towers are shadowed by the BCAL, they are programmed so they do not set bits for isolated electrons themselves, but can contribute "quiet" bits to the pattern logic. The FCAL EMC sections that are shadowed by BCAL EMC sections are combined with the BCAL EMC sections at the BCAL TEC front ends. The other HAC0 towers not inside the 7 x 8 groups contribute to the hadronic sections of the forward BCAL supertowers. Crates 4 - 7 cover the RCAL in a similar manner.

In the BCAL, there are 32 modules, each covering a ϕ slice and having 14 sections along the beampipe direction. Each of the 8 BCAL Trigger Crates (8 - F hexadecimal) covers either the front or back 7 sections of 8 BCAL modules. The 16 Trigger Crates are assigned to the regions of the FCAL, BCAL and RCAL as shown in Figure 19. Also shown are the edge definitions. These edges are numbered as used by the pattern logic, which counts the number of candidate isolated electrons and muons individually on edges 0 through 3. This number is reported to the Trigger Processor, which then checks the appropriate neighboring edge in the adjoining region. The pattern logic also sends back a bit indicating whether each of the 4 edges was quiet (i.e. had only Q, M or E bits set).

In the event it is necessary to stage the installation of the calorimeter trigger, combinations of supertowers will be made to reduce the total amount of Trigger Crates required in the Rucksack. Since the most difficult triggering situation is found in the FCAL, no combinations will be made there. The Trigger Crates in the BCAL will cover twice the range in ϕ as the final configuration. This yields four total Trigger Crates after combining 8 with 9, A with B, C with D, and E with F. One Trigger Crate will be used in the RCAL in the place of the four of the final system. The calorimeter trigger system is designed to be able to adiabatically evolve from the staged to final system through reprogramming of the memory lookup tables and recabling the TEC front ends.

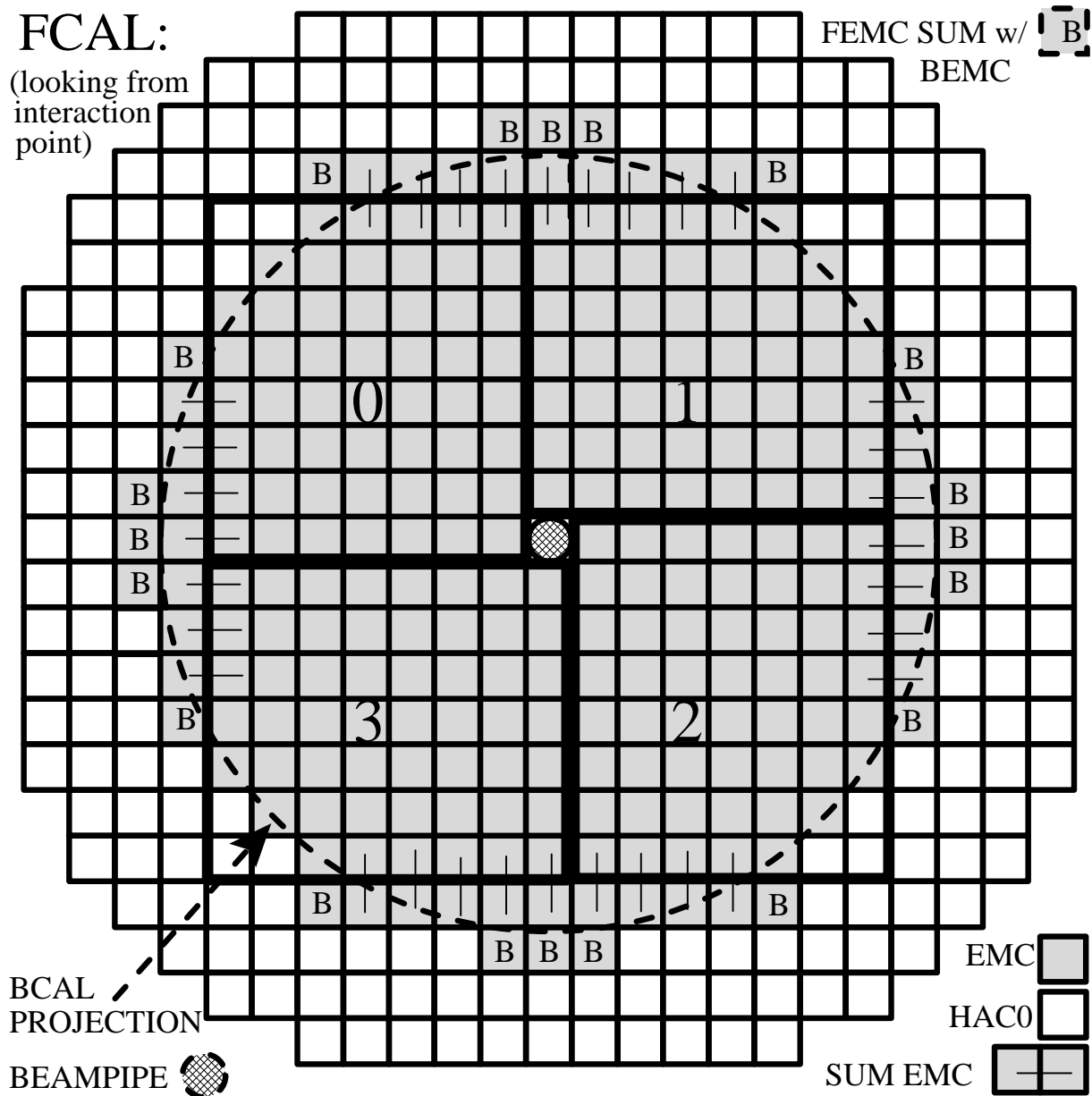


Figure 18. Organization of Trigger Supertowers in the FCAL. The front face of the FCAL is shown. EMC sections are grey, HAC0 sections are white. FCAL EMC sections that are combined with other FCAL EMC sections are linked together. FCAL EMC sections that are summed with BCAL EMC sections as part of BCAL supertowers are labelled with a "B".

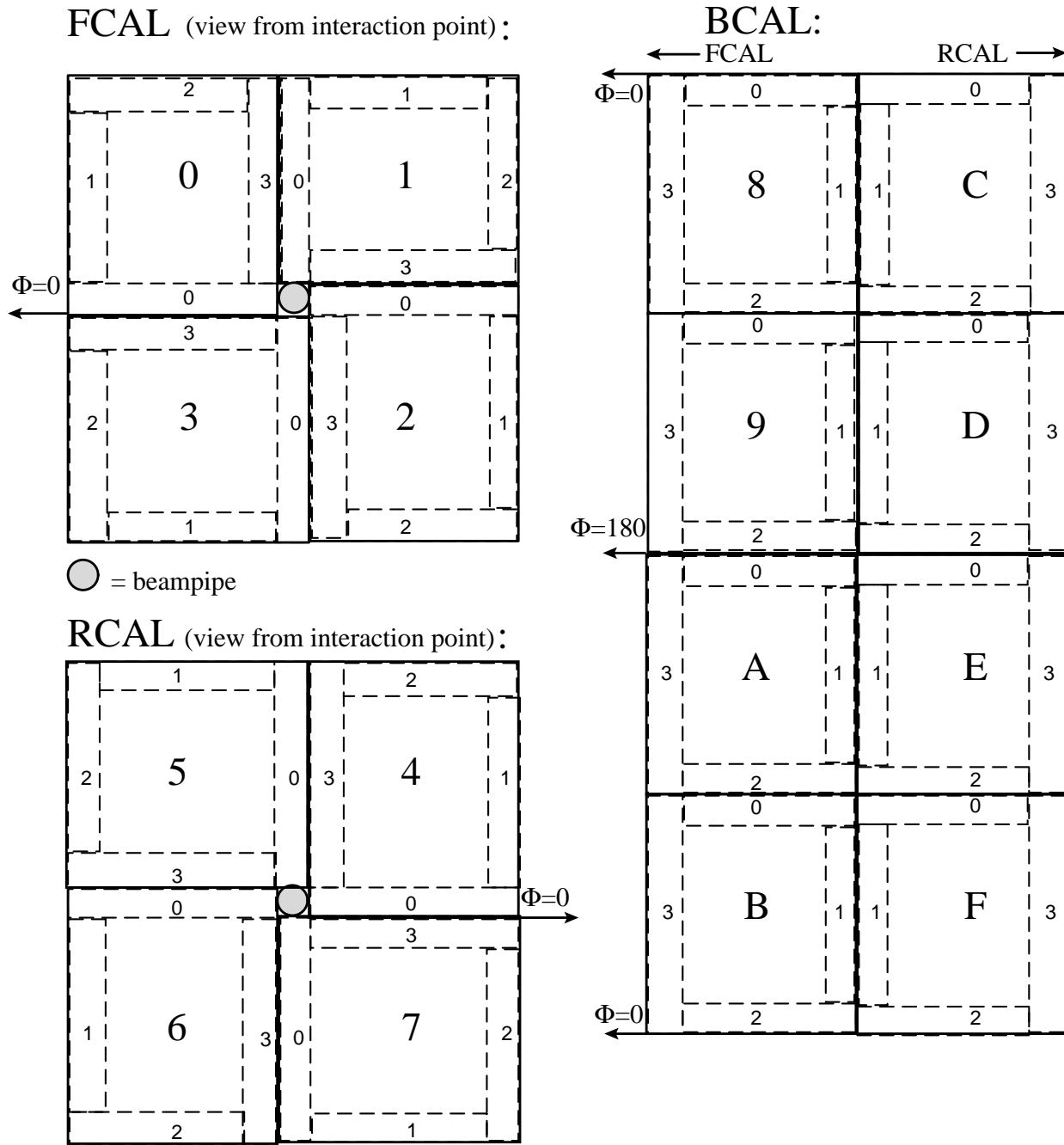


Figure 19. Organization of Trigger Crates in the Calorimeter. The assignment of edges for each region serviced by a Trigger Crate is shown.

Figure 20 shows the same distribution of regions assigned to Trigger Crates as in Figure 19, but with the subregions marked. The Adder Cards determine the energy within these subregions by summing the threshold bits from the individual supertowers. The subregions are chosen so that the Trigger Processor can reconstruct the beam-gas energy in the FCAL with several different radii from the beam-pipe. The subregions are designed to cover areas in θ - ϕ space. The boundary between FCAL and BCAL, as well as between BCAL and RCAL, is also covered by special subregions so that the Trigger Processor can reconstruct the energy deposited in this boundary region. Since this is the area where the geometry is most problematical, the Trigger

Processor may change cut requirements for events with a significant deposit of energy in this region.

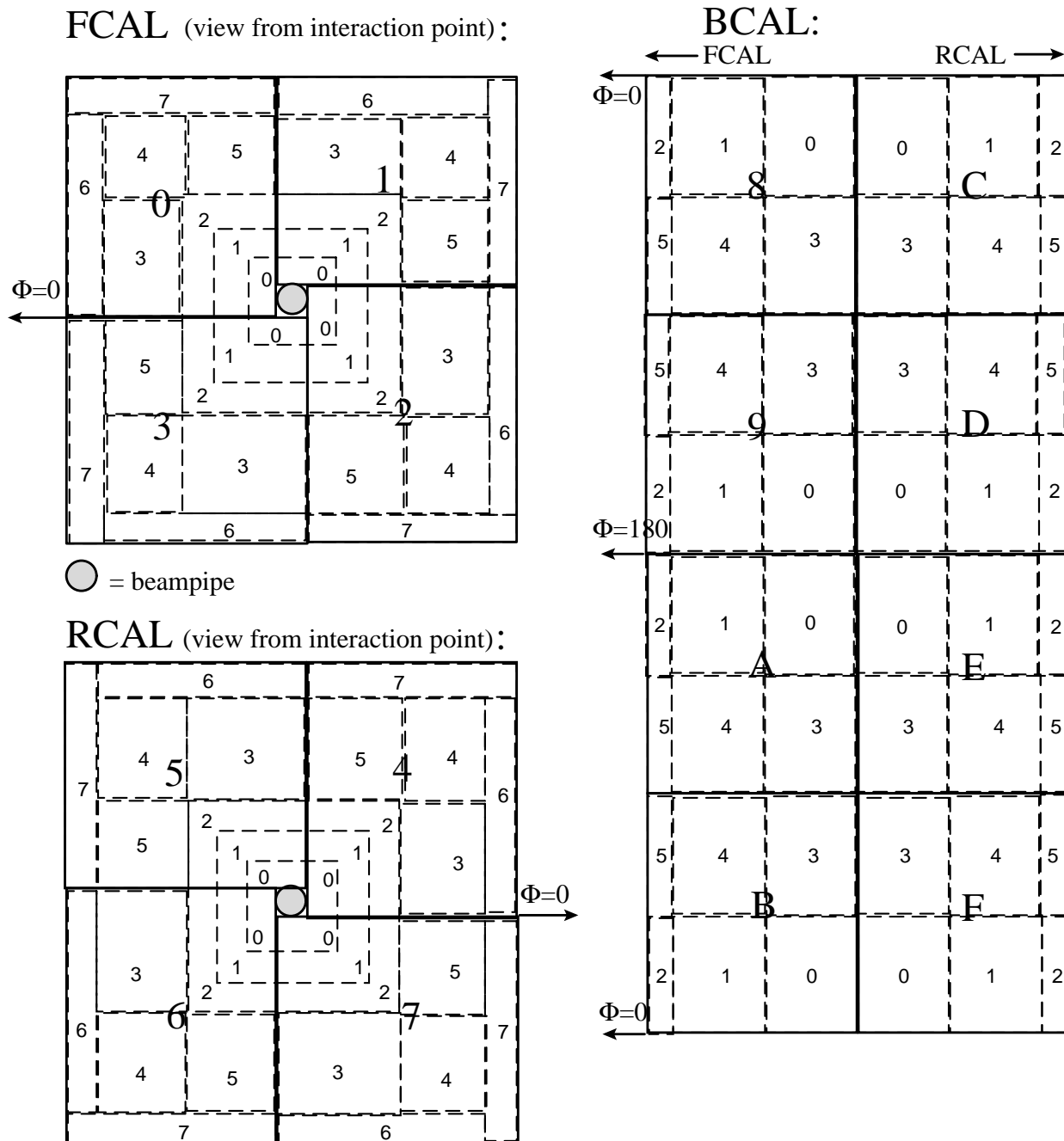


Figure 20. Organization of Trigger Crates in the Calorimeter. The assignment of subregions for each region serviced by a Trigger Crate is shown.

The assignment of individual EMC and HAC towers to trigger towers is based on the projection of the EMC towers back into the HAC sections. The EMC towers are composed of 4 roughly 5 cm x 20 cm sections in the FCAL and BCAL, and 2 roughly 10 cm x 20 cm sections in the RCAL. The most forward and most rear BCAL EMC towers have 2 and 3 sections respectively. In the FCAL, there are 28 trigger supertowers where 2 EMC towers are summed together, and 12 trigger supertowers where 3 EMC towers are summed together. As shown in

Figure 18, these EMC towers are the most distant from the beampipe, and partially covered by the projection of the BCAL EMC sections. A side view of the assignment of the trigger supertowers is shown in Figure 21. There are some FCAL and RCAL HAC towers that are "shadowed" by BCAL EMC towers. These are assigned to BCAL trigger supertowers as shown in Figure 21.

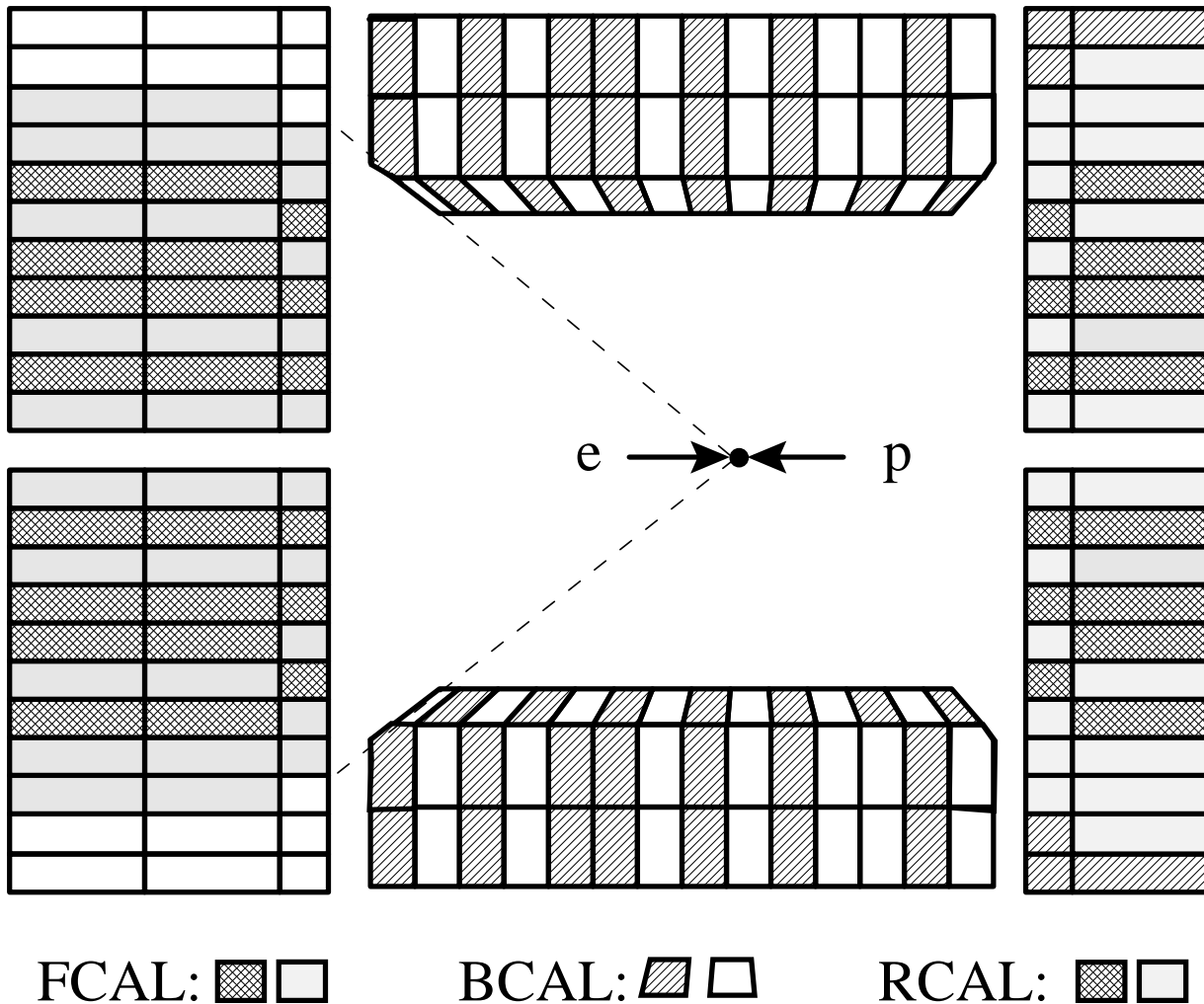


Figure 21. Assignment of Trigger Supertowers shown in alternating patterns separately for the FCAL, BCAL and RCAL. HAC towers assigned to supertowers with BCAL EMC towers are shown as part of BCAL supertowers.

The individual Trigger Crates have split backplanes, which are labelled left and right. The Adder Cards in each crate alternate reading in threshold bits and the {Q,M,E} bits. Each Adder Card sends bits from the cards on its half backplane to the Adder Card on the other half-backplane once cycle after receiving them. In order for the pattern logic to receive the supertower data in the appropriate sequence, the TEC's must be connected so that towers that must follow each other in the pattern logic, must alternate between the left and right backplanes. This connection of TEC channels to FCAL supertowers is shown in Figure 22. Here the supertowers in the four 7 x 8 regions shown in Figure 18 are assigned to TEC channels. The Trigger Crate number and attachment to either right or left backplane is indicated on the side of the region. In

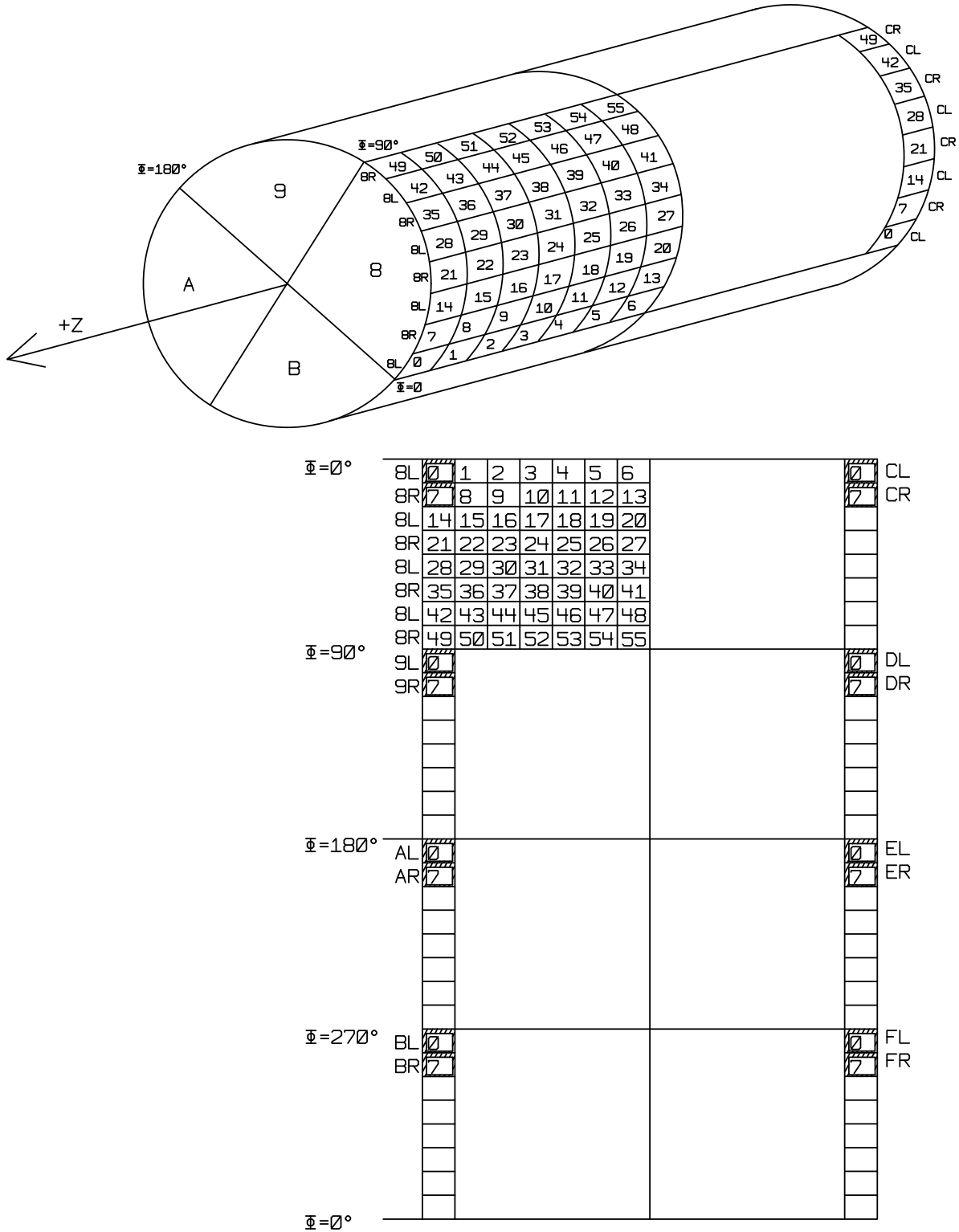


Figure 23. Organization of Supertowers in the BCAL Trigger Crates.

15. Trigger Processor Crate

The Calorimeter First Level Trigger Processor (CFLTP) does the final trigger calculations with data from the Master Adder Cards and ships these results to the Global First Level Trigger (GFLT) for the final trigger decision. The Master Adder Cards send the number of contained isolated electrons, edge isolated electrons, contained isolated muons and edge isolated muons. The edge counts are also broken down into totals for each of the 4 edges of the 56-supertower region. The Adder Cards also send the number of supertowers that exceeded each (or no) threshold, but not the next higher threshold, number that overflowed their low gain channel, and whether these overflows are corrected for by setting the energy of their channel to zero.

The Adder Cards send the energy in 8 specific subregions of the 56-supertower region as calculated from the supertowers passing the thresholds. The total energy in the 56-supertower region calculated from these thresholds is also sent. The initially planned subregions include beam-gas, region edges, and region interior (contained). These are presented in the section on Assignment of Trigger Crates and Supertowers. The total edge energy and energy not in the beam-gas region are extracted by the CFLTP by subtracting the contained energy and the beam-gas energy from the total energy calculated from the threshold tests. The Adder Cards also send the EMC and HAC 56-supertower sums of total energy and transverse energy, E_x and E_y .

The Trigger Processor produces information on the global and regional status of the calorimeter trigger. It indicates for each of the 16 regions whether there was an electronic overflow and whether this overflow was corrected for by adding in zero energy. The Trigger Processor counts the total number of isolated muons and isolated electrons. These sums are made by first adding all of the contained isolated muons and electrons. The edge muons and electrons are matched up with the appropriate edge of the neighboring 56-supertower region. If the adjoining edge is quiet or has an isolated edge electron or muon in it, a single isolated electron or muon is included in the sum. If the adjoining edge is neither quiet nor contains an isolated muon or electron, the isolated muon or electron is not counted.

The Trigger Processor completes the summation of total, HAC, and EMC energy and transverse energy, E_x and E_y . These sums are made with 8-bit accuracy. The total missing energy ($E_x^2 + E_y^2$) and the total missing electromagnetic energy are also directly calculated. The total, transverse and x and y components of total, EMC and HAC energy are compared against settable thresholds and the results are forwarded to the GFLT. The same is done for the total and EMC missing energy. These thresholds will be scattered through the dynamic range to correspond to the amounts of energy required for triggering when correlated with and without other components.

The Trigger Processor calculates the sum of the energy contained in the beam-pipe region of the FCAL and the RCAL and the ratio of HAC energy to EMC energy in the RCAL. This ratio is expected to be high for beam-gas supertowers entering the back of the RCAL. Other useful beam-gas information provided includes a global BCAL EMC sum, and an indication whether any supertower had an energy over the maximum kinematically possible. The Trigger Processor determines a beam-gas score representing the result of an algorithm that uses the information above with the energy sums to create a probability that the energy observed is due to beam-gas interactions.

The number of isolated electrons and muons found in the detector is the sum of the contained isolated electrons and muons and the verified edge isolated electrons and muons. The totals of contained isolated muons and electrons within 56-supertower regions are reported by the Adder Cards. Edge isolated electrons and muons in a specific 56-supertower region are verified by checking the edge region of the adjacent 56-supertower region for another edge isolated isolated electron or muon, or all "quiet". In the case where another isolated electron or muon is

found, the two neighboring edge isolated electrons or muons are combined and counted as a single contained isolated electron or muon. In the case where the edge region adjoining an edge isolated electron or muon is "quiet", the edge isolated electron or muon is counted as a single contained isolated muon or electron. In the case where the adjacent edge region is neither "quiet" nor contains an isolated electron or muon, the edge isolated electron or muon is rejected.

A potential difficulty with electron identification is the susceptibility of the electron test to PMT discharge or other noise. This is because the electron test depends on a deposition of energy in a single EMC tower with remaining towers relatively quiet. An individual PMT discharge would effect either the right or left EMC PMT, but not both. Since the left and right PMT's are summed at the TSC, the information arriving at the TEC does not permit this check. The solution, described in the section on the TSC, is to check whether the right and left PMT's are both above or below a settable threshold at the TSC before summing. Failure of this test results in the setting of the veto bit from the TSC. These veto bits are OR'ed for all HAC and EMC channels in a half calorimeter module and sent to the Trigger Processor directly. The Trigger Processor deglitches these signals and correlates them with the appropriate CAL FLT regions, where they are used to veto electron (and other, if necessary) triggers due to noise.

The Trigger Processor also searches for clusters of energy using the regional sums. Contained energy with small edge energy is treated as a cluster. Two adjacent edges with small energy in adjacent contained regions are treated as clusters. The contained energy or the sum of the two combined edges becomes the cluster energy. The energy of these clusters is checked against three thresholds and the number of clusters with energy greater than each of the three thresholds is sent to the GFLT. Further information contains E_x and E_y for the HAC sums, EMC sums and HAC + EMC sums. Information is provided on the regional number of isolated electrons and isolated muons (verified edge depositions are reported in both regions), amount of total energy transverse energy, amount of energy in the beam-gas subregion of the region (i.e. part closest to the beam-pipe), and the amount of electromagnetic energy. The Trigger Processor is described in detail in Zeus-Note-89-086.

16. Communication: Adder Card to Trigger Processor

The 16 Master Adder Cards send data from each of their crates to the Trigger Processor Crate on four 17-pair twist-and-flat cables with 24 nsec clocking, yielding four words per cable every 96 nsec. On each cable, the data is in the lower 16 bits and a timing marker is placed in the 17 bit. The first word of the first cable has the lowest 4 bits of the crossing number in its lowest 4 bits, it then has 4 3-bit words with the number of contained isolated electrons, edge isolated electrons, contained isolated muons and edge isolated muons. The second word has a 6-bit and 2 5-bit words counting the number of supertowers that passed no threshold, the first threshold (but not the second), and the second threshold (but not the third), respectively. The third word has 4 4-bit words counting the number of supertowers that passed the the third threshold (but not the fourth), fourth threshold (but not the fifth), the fifth threshold (but not the sixth), and the sixth threshold (but not an overflow). The fourth word contains a 4-bit word counting the number of overflow supertowers, one bit indicating whether these overflows were corrected for by setting the output of the overflow channel to zero, one bit indicating a trigger error and a 10-bit word with the total energy in the 56-supertower region as calculated from the supertowers passing the thresholds.

The second cable contains 4 16-bit words divided into 8 bits apiece with the energy in a specific subregion of the 56-supertower region as calculated from the supertowers passing the thresholds. There are 8 of these total subregion supertower sums available. These subregions are

defined in the section on Assignment of Trigger Crates and Supertowers. The definitions of these subregions may be changed under software control.

The third cable contains the EMC and HAC 56-supertower sums of total energy and transverse energy in the bits 4 through 12 of 4 16-bit words. The lower 4 bits of these words contain the number of isolated electrons in the lowest 2 bits and the number of isolated muons in the higher two bits for edges 0, 1, 2 and 3 respectively. These edges are defined in the section on Assignment of Trigger Crates and Supertowers.

The fourth cable contains the EMC and HAC 56-supertower sums of E_x and E_y in bits 4 through 12 of 4 16-bit words. The lowest two bits of the 4 words contain the clock phase, which counts 0 through 3 in the first through fourth words. The next 2 bits of the first word contain, from bit 2 through bit 3, a bit indicating whether edges 0 and 1 were quiet, respectively. Similarly, in the second word bits 2 and 3 indicate whether edges 2 and 3 were quiet, respectively. The bits 2 and 3 of the last 2 words are reserved for future use. The cable assignments are shown in Table 5.

Table 5. Cable assignments for communication from Master Adder Cards to the CFLTP.

WORD: BIT:	CABLE 1			
	FIRST (0 ns)	SECOND (24 ns)	THIRD (48 ns)	FOURTH (72 ns)
0	Crossing No.	S'twrs < T1	T3 < S'twrs < T4	Overflow S'twrs
1	" "	" "	" "	" "
2	" "	" "	" "	" "
3	" "	" "	" "	" "
4	Contained e's	" "	T4 < S'twrs < T5	Overflow Correct
5	" "	" "	" "	Trigger Error
6	" "	T1 < S'twrs < T2	" "	E_{TOT} from Thresh.
7	Contained μ 's	" "	" "	" "
8	" "	" "	T5 < S'twrs < T6	" "
9	" "	" "	" "	" "
10	Reserved	" "	" "	" "
11	" "	T2 < S'twrs < T3	" "	" "
12	" "	" "	T6 < S'twrs < OV	" "
13	" "	" "	" "	" "
14	" "	" "	" "	" "
15	" "	" "	" "	" "

CABLE 2

WORD:	FIRST (0 ns)	SECOND (24 ns)	THIRD (48 ns)	FOURTH (72 ns)
BIT:				
0	Subreg. 0 Egy.	Subreg. 2 Egy.	Subreg. 4 Egy.	Subreg. 6 Egy.
1	" "	" "	" "	" "
2	" "	" "	" "	" "
3	" "	" "	" "	" "
4	" "	" "	" "	" "
5	" "	" "	" "	" "
6	" "	" "	" "	" "
7	" "	" "	" "	" "
8	Subreg. 1 Egy.	Subreg. 3 Egy.	Subreg. 5 Egy.	Subreg. 7 Egy.
9	" "	" "	" "	" "
10	" "	" "	" "	" "
11	" "	" "	" "	" "
12	" "	" "	" "	" "
13	" "	" "	" "	" "
14	" "	" "	" "	" "
15	" "	" "	" "	" "

CABLE 3

WORD:	FIRST (0 ns)	SECOND (24 ns)	THIRD (48 ns)	FOURTH (72 ns)
BIT:				
0	Edge 0 Isol. e's	Edge 1 Isol. e's	Edge 2 Isol. e's	Edge 3 Isol. e's
1	" "	" "	" "	" "
2	Edge 0 Isol. μ 's	Edge 1 Isol. μ 's	Edge 2 Isol. μ 's	Edge 3 Isol. μ 's
3	" "	" "	" "	" "
4	EMC E_{TOT}	HAC E_{TOT}	EMC E_T	HAC E_T
5	" "	" "	" "	" "
6	" "	" "	" "	" "
7	" "	" "	" "	" "
8	" "	" "	" "	" "
9	" "	" "	" "	" "
10	" "	" "	" "	" "
11	" "	" "	" "	" "
12	EMC E_{TOT} Overflow	HAC E_{TOT} Overflow	EMC E_T Overflow	HAC E_T Overflow
13	Reserved	Reserved	Reserved	Reserved
14	" "	" "	" "	" "
15	" "	" "	" "	" "

CABLE 4				
WORD:	FIRST (0 ns)	SECOND (24 ns)	THIRD (48 ns)	FOURTH (72 ns)
BIT:				
0	Clock Phase	Clock Phase	Clock Phase	Clock Phase
1	" "	" "	" "	" "
2	Quiet Edge 0	Quiet Edge 1	Reserved	Reserved
3	Quiet Edge 2	Quiet Edge 3	" "	" "
4	EMC E _X	HAC E _X	EMC E _Y	HAC E _Y
5	" "	" "	" "	" "
6	" "	" "	" "	" "
7	" "	" "	" "	" "
8	" "	" "	" "	" "
9	" "	" "	" "	" "
10	" "	" "	" "	" "
11	" "	" "	" "	" "
12	Ignore	Ignore	Ignore	Ignore
13	Reserved	Reserved	Reserved	Reserved
14	" "	" "	" "	" "
15	" "	" "	" "	" "

The Trigger Processor Crate sends a single cable made of 8 individually shielded differentially driven twisted pairs to each Master Adder Card. The first pair carries the 96 nsec clock from the GFLT, which is sent through the Trigger Crate as 96CLK. The Trigger Processor receives this signal from the GFLT on pair 5 of the GFLT Clock Cable. The second pair is unused. The third pair carries a 12 nsec ECL clock produced by subdivision of the 96 nsec clock. The fourth pair also is unused. The two unused pairs are present to provide additional signal shielding. The fifth pair carries the Crossing 0 indicator from the GFLT, which is carried on GFLT Clock Cable pair 6. The sixth and seventh pairs carry the GFLT Readout Type, which are carried on GFLT Control Cable pairs 6 and 7. The eighth pair carries the Trigger Accept Signal from the GFLT, which is found on pair 14 of the GFLT Control Cable. A Trigger Accept signal accompanied by both bits zero of the GFLT Readout Type constitutes a First Level Trigger signal. A Trigger Accept signal accompanied by both GFLT Readout Type bits set to one constitutes an initialize command. Additional details on the GFLT information are found in Zeus memo 88-098.

Table 6. Cable assignments for communication from CFLTP to the Master Adder Cards.

BIT:	CONTENTS:	BIT:	CONTENTS:
0	96 nsec clock	4	Crossing Zero
1	Ground (for Shielding)	5	GFLT Readout Type
2	12 nsec clock	6	" "
3	Ground (for Shielding)	7	GFLT Accept

17. Global First Level Trigger

The calculations of the Trigger Processor take 2 μ sec to complete. The results from the Trigger Processor are shipped to the Global First Level Trigger (GFLT) that combines different detector elements for a final trigger decision in 5 μ sec. A typical example is to require an $E_T > 10$ GeV in the CAL accompanied by a Central Tracking Detector (CTD) multiplicity > 5 tracks pointing at the interaction point. The GFLT is also pipelined, accepting data and sending a decision every 96 nsec. Due to propagation delays in receiving the data and sending the trigger, the GFLT calculation time is also 2 μ sec. After the issuing of the GFLT, the event is analyzed by the Second Level Trigger. This system can handle a rate of 1 kHz.

The GFLT can also correlate regional information from detector elements such as the CTD and the CAL to make its decisions. This may be done by the GFLTB itself or by a separate correlation circuit. Three such correlations are described here. The CTD information would be grouped in 16 regions to match the CAL trigger system. The CTD would provide the multiplicity of tracks in 3 bits, whether the tracks were well measured in one bit, and whether the track pointed at the interaction point in a bit. A track that is not well measured only intersects a single superlayer of the CTD and hence its pointing at or away from the interaction point is not well known. These total 5 CTD regional bits would be combined with the CAL regional information including 2 bits each counting the number of isolated electrons and muons, and 3 bits giving the electromagnetic energy in the region. The result would be the number of isolated muons and electrons gated on CTD information indicating a track pointing at the vertex. A second correlation would be to combine the 5 regional CTD bits with the CAL regional information including 3 bits of the sum of transverse energy, 3 bits of beam-gas subregion energy and 3 bits of total energy to produce a transverse energy sum gated on CTD and CAL beam-gas indicators. A third correlation would be to combine the 5 regional CTD bits with the CAL regional information including the number of supertowers in 3 bits apiece passing the sixth, fifth and fourth energy thresholds. This would constitute a crude jet trigger.

18. Communication to Fast Clear

The contents of one address on each of the 8 64x9 FIFO's on the Trigger Encoder Card are transferred to 8 9-bit registers upon receipt of a GFLT. This address is preselected to correspond to data from the beam crossing which produced the GFLT. The GFLT is detected on the Trigger Encoder Card by checking that the backplane lines which carry GFLT Accept = 1, and both Readout Type bits = 0. These signals are carried from the GFLTB through the CFLTP to the Adder Card, which places them on dedicated lines on the backplane. When the GFLT is detected, the 64x9 FIFO's do not stop clocking forward, but transfer the data from the appropriate position into the registers that serve as a one-event-buffer. This data contains 8 bits of energy and one bit of scale. If the scale bit is 0, the scale is 12.5 GeV/256 per bit. If the scale bit is 1, for FCAL the scale is 400 GeV/256 per bit, and for BCAL and RCAL the scale is 100 GeV/256 per bit. The scales are selected so that with the scale bit set the data is shifted up 5 bits (x32) for FCAL, and 3 bits (x8) for BCAL and RCAL.

The detection of a GFLT also initiates the sending of data from the 9-bit registers to the Fast Clear. Each half of the split J2 bus in the Trigger Crate has nine lines on it reserved for this purpose. These lines are brought out on four 9-pair cables per crate. There are two cables for each split J2 bus, one carries the HAC data and the other carries the EMC data. Only one of the 7 Trigger Encoder Cards connected to the half of the backplane places one of its supertower's HAC and EMC data on the 18 total lines at any one time.

The Fast Clear communicates with the Calorimeter First Level Trigger (CAL FLT) with HOLD and VALID signals. When the Fast Clear is working on an event, it asserts a HOLD. When the Fast Clear is finished and can accept a new event, it releases the HOLD. Upon receipt of a GFLT, the CAL FLT waits for the HOLD from the Fast Clear to be lifted. When it is lifted, the CAL FLT asserts a VALID on the next 24 nsec clock cycle. The first data words from the CAL FLT to the Fast Clear are sent on the 24 nsec clock cycle directly following the raising of the VALID signal. After the Fast Clear lifts its HOLD, the receipt of a VALID signal from the CAL FLT sets the Fast Clear to start receiving 9-bit words on the next 24 nsec clock cycle. The CAL FLT indicates the end of the data by lowering the VALID signal. The Fast Clear will immediately raise its HOLD signal when the CAL FLT lowers its VALID. If a GFLT is issued before the Fast Clear has finished processing an event, the Fast Clear will immediately cease

processing, clear its front end memories, and lift its HOLD signal. In this case, the wait for the HOLD release will be longer than in the case where the Fast Clear has already finished and reset.

Appendix A: VME Address Space Mapping.

The list below details the assignment of bits in the VME address space as they apply to the Trigger Encoder Card.

Top 5 bits (19-23):	Board Address
Next 2 bits (17-18):	An encode of memory TYPE as defined in the text. 00 = LINM, 01 = GMA, 10 = GMB, 11 = TSTM
Next 3 bits (14-16):	TOWER number 000 = Tower 1, HAC; 001 = Tower 1, EMC 010 = Tower 2, HAC; 011 = Tower 2, EMC 100 = Tower 3, HAC; 101 = Tower 3, EMC 110 = Tower 4, HAC; 111 = Tower 4, EMC
Next 13 bits (1-13):	Address bits for memories and registers
LSB (0):	Ignored
Command register:	Type = 3, Tower = EMC, address = four LSB's = 000X
FIFO countdown:	Type = 3, Tower = EMC, address = four LSB's = 001X
Programmable delay:	Type = 3, Tower = EMC, address = four LSB's = 010X

The list below shows the actual assignment of binary values on the VME address lines as they are used for writing the various registers and memories in the trigger encoder card. The "b" stands for the appropriate binary value, such as a bit that is part of a card or memory address. The "x" stands for a bit whose value is ignored.

COMMAND	bbbb b11x x1xx xxxx xxxx 000x
FIFO COUNTER	bbbb b11x x1xx xxxx xxxx 001x
DELAY	bbbb b11x x1xx xxxx xxxx 010x
TOWER 1, HAC, LINM	bbbb b000 00bb bbbb bbbb bbbx
TOWER 1, EMC, LINM	bbbb b000 01bb bbbb bbbb bbbx
TOWER 2, HAC, LINM	bbbb b000 10bb bbbb bbbb bbbx
TOWER 2, EMC, LINM	bbbb b000 11bb bbbb bbbb bbbx
TOWER 3, HAC, LINM	bbbb b001 00bb bbbb bbbb bbbx
TOWER 3, EMC, LINM	bbbb b001 01bb bbbb bbbb bbbx
TOWER 4, HAC, LINM	bbbb b001 10bb bbbb bbbb bbbx
TOWER 4, EMC, LINM	bbbb b001 11bb bbbb bbbb bbbx
TOWER 1, HAC, GMA	bbbb b010 00bb bbbb bbbb bbbx
TOWER 1, EMC, GMA	bbbb b010 01bb bbbb bbbb bbbx
TOWER 2, HAC, GMA	bbbb b010 10bb bbbb bbbb bbbx
TOWER 2, EMC, GMA	bbbb b010 11bb bbbb bbbb bbbx
TOWER 3, HAC, GMA	bbbb b011 00bb bbbb bbbb bbbx
TOWER 3, EMC, GMA	bbbb b011 01bb bbbb bbbb bbbx
TOWER 4, HAC, GMA	bbbb b011 10bb bbbb bbbb bbbx
TOWER 4, EMC, GMA	bbbb b011 11bb bbbb bbbb bbbx
TOWER 1, HAC, GMB	bbbb b100 00bb bbbb bbbb bbbx
TOWER 1, EMC, GMB	bbbb b100 01bb bbbb bbbb bbbx
TOWER 2, HAC, GMB	bbbb b100 10bb bbbb bbbb bbbx
TOWER 2, EMC, GMB	bbbb b100 11bb bbbb bbbb bbbx
TOWER 3, HAC, GMB	bbbb b101 00bb bbbb bbbb bbbx
TOWER 3, EMC, GMB	bbbb b101 01bb bbbb bbbb bbbx
TOWER 4, HAC, GMB	bbbb b101 10bb bbbb bbbb bbbx
TOWER 4, EMC, GMB	bbbb b101 11bb bbbb bbbb bbbx
TOWER 1, TSTM	bbbb b110 00bb bbbb bbbb bbbx
TOWER 2, TSTM	bbbb b110 10bb bbbb bbbb bbbx
TOWER 3, TSTM	bbbb b111 00bb bbbb bbbb bbbx
TOWER 4, TSTM	bbbb b111 10bb bbbb bbbb bbbx